INTEGRATED SILICON SOLUTION, INC.

2009 Quality and Reliability Manual

Telematics Systems

Lane Warning Departure Systems

Back-up Camera Systems

Night Vision Systems

Radio and Audio Systems

Satellite Radio

DVD Players and Rear Seat Entertainment

Navigation Systems

Body Control Electronics

Gateway

Clusters Dashboard

Transmission Control

Engine Controls

Hybrid Battery Monitoring/Charging

Contents

Contents i

Chapter 1 Quality Management 1
1.1 Quality Policy 1
1.2 Quality Organization 1
1.3 ISO 9001 Year 2000 Revision 2
1.4 Quality Systems 4
1.4.1 Process Map 4
1.4.2 Advanced Product Quality Planning 6
1.4.3 Quality Assurance in the Project Approval Stage 7
1.4.4 Quality Assurance in Design Development Stage 7
1.4.4.1 Product Development and Design 7
1.4.4.2 Design Review 7
1.4.4.3 Product Release 8
1.4.4.4 Production Part Approval Process (PPAP) 8
1.4.5 Quality Assurance in Production Stage 8
1.4.5.1 Wafer Processing 8
1.4.5.2 Assembly Process 11
1.4.5.3 Testing 13
1.4.5.4 Known Good Die flow 18
1.4.6 Quality Assurance of Product Shipping 20
1.5 Change Control 21
1.6 Customer Complaint 23
1.6.1 ISSI RMA Process 23
1.6.2 ISSI RMA Flow 24
1.7 e-CAR 25
1.7.1 Corrective Action 25
1.7.2 Preventive Action 25

Chapter 2 Management on Subcontractors 28
2.1 Task Force 28
2.2 Methodology 28

2.3 Quality Rating 29
2.4 Supplier Relationship 30

Chapter 3 Product Reliability 31
3.1 Reliability Assurance 31
3.1.1 Product/Process Qualification 31
3.1.2 Qualification Test Method and Acceptance Criteria 36
3.1.3 Semiconductor Device Failure Region 41
3.1.4 Failure Rate Calculation 42
3.1.5 Philosophy of Reliability Monitor 48
3.1.6 Reliability Test Equipment List 50
3.2 Device Related Test Data 54
3.3 Package Related Test Data 58
3.4 Lead-Free Package Roadmap 58
3.5 Process Average Testing (PAT), Statistical Yield Analysis (SYA) And Junction Verification Test (JVT) 60

Chapter 4 Failure Analysis 65
4.1 Establishment of Failure Analysis (FA) Laboratory 65
4.1.1 Electrical Failure Analysis (EFA) Laboratory 65
4.1.2 Assembly Engineering and Chemical Laboratory 65
4.1.3 Physical Failure Analysis (PFA) Laboratory 65
4.2 Failure Analysis Function 66
4.3 Failure Analysis Flow 67
4.4 Failure Analysis Instruments 69

Chapter 5 Environmental Management 74
5.1 Environmental Policy 74
5.2 Environmental Management Quality Assurance 75
5.2.1 ISO14001 Certificate - Taiwan 76
ISO14001 Certificate – China 77
5.2.2 Environmental Management Organization 78
5.3 Environmental Substances Management 78
5.3.1 Green Partner Certification 80
5.3.2 Legislation and SONY Policy 80

5.3.3 Industry Definition of Lead-free & Halogen-free 81
5.3.4 Product Composition 82
5.3.5 Lead-free Solution 83
5.3.6 Halogen-free Solution 86
5.3.7 Pb-free/Halogen-free Evaluation/Qualification Information 87
5.3.8 Current Status 90
5.3.9 Solder Heat Resistance for PCBA (PC Board Assembly) 91
5.3.10 Lead Time from Ordering to Delivery 91
5.3.11 Discrimination Mark of Lead-free and RoHS Compliance Package 91
5.3.12 ISSI Declaration of Compliance 92

Appendices

Contents

1 IR Re-flow Temperature Profile for Lead-free Package 93

2 Recommended Storage Condition 94

3 Milestones and Awards 95

4 Data

4..1.1 Table 1-1 AOQL (SRAM) 96

4.1.2 Table 1-2 AOQL(DRAM) 97

4.1.3 Table 1-3 AOQL (EEPROM) 98

4.1.4 Table 1-4 OQC LRR Trend Chart 99

4.1.5 Table 1-5 Visual Mechanical Check 100

4.2.1 Table 1-6 RMA's by Month 101

4.2.2 Table 1-7 RMAs by Product Type 102

4.3 Device Related Test Data 103

Table 1-9 FIT Value for product of SRAM, DRAM, and LOGIC 103

Table 1-10 High Temperature Operation Life Test 106

Table 1-11 Electrostatic Discharge (ESD) and Latch-up Tests 120

Table 1-12 Data Retention 131

Table 1-13 Endurance Cycling and Data Retention Tests 132

4.4 Package Related Test Data 134

Table 1-14 Pre-condition Test 134

Table 1-15 Highly Accelerated Stress Test 149

Table 1-16 Temperature Cycling Test 165

Table 1-17 Pressure Cooker Test 181

Table 1-18 Device Monitor Qual – 168 Hrs HTOL 197

4.5 Failure Analysis Cases 201

4.5.1 Example of FA Case - SRAM (0.35 µm, 3P2M) 201

4.5.2 Example of FA Case - DRAM (0.18 µm, 4P2M) 202

4.5.3 Example of FA Case - Logic (0.25 µm, 1P5M) 203

4.6 Construction Analysis 204

4.6.1 0.15 µm 6T SRAM (A015) 204

4.6.2 0.099 µm Synchronous DRAM (K018) 206

4.6.3 0.25 µm 4T SRAM (A006) 208

Chapter 1 Quality Management

1.1 Quality Policy

ISSI Management and all other team members are committed to:

* understand and satisfy customer needs
* provide defect-free products cost effectively
* continuously improve our methods and processes
* training that supports our quality values
* be the best in class in everything we do

1.2 Quality Organization

ISSI headquarters is located at 1940 Zanker Road, San Jose California USA where the corporate policies and programs are determined and applied to world-wide operations. The Taiwan facility is located in the Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C. The China facility is located in Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai. Operations in Taiwan and China consist primarily of research and development activities and Foundry and Subcontractor management. Subcontracted operations include wafer fabrication, assembly and final test. Many of these subcontractors are located in Taiwan and China and are managed by Taiwan and China quality organization. The Quality Organization is outlined in Figure 1-1.

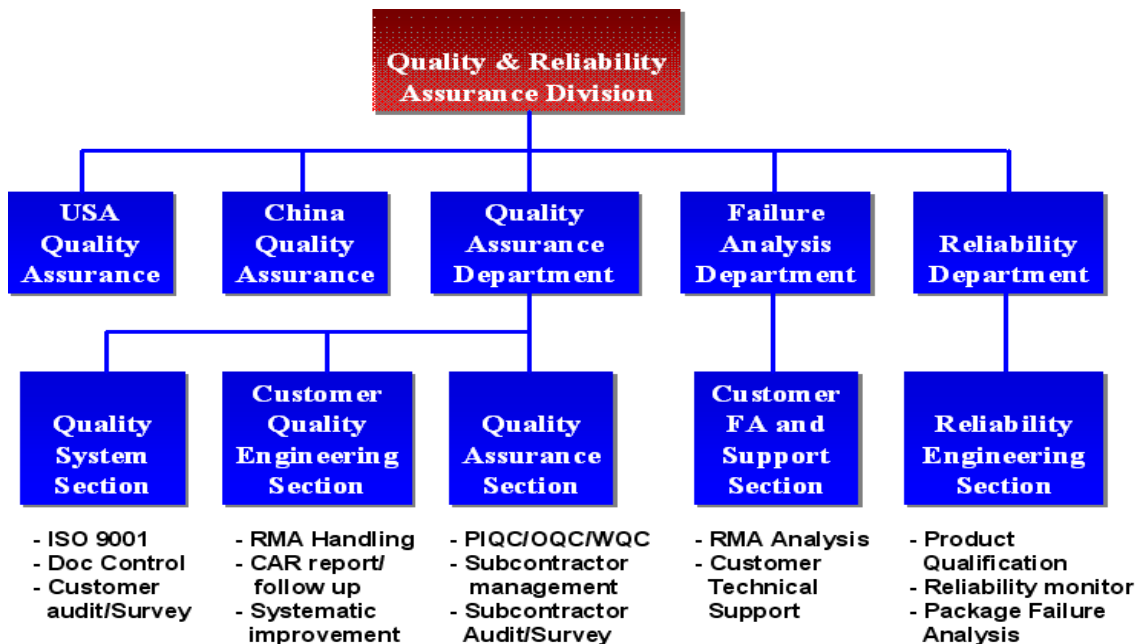


Figure 1-1 ISSI Quality Organization

1.3 ISO 9001 Year 2000 Revision

The Management team has defined the quality policy and objectives for ISSI and has established a quality management system to ensure that the quality policy and quality objectives are understood, implemented and maintained. The Quality System defined in ISSI Quality Manual is in compliance with the requirements of ISO 9001: 2000. It is stratified and compiled into documents with quality manuals at the top supported by procedures, specifications, regulations, rules and detailed work instructions, etc (see Figure 1-2).

Employees are trained and keep records of duties carried out according to the prescribed methods based on the latest documents to ensure that the constructed quality system is implemented in the prescribed manner.

The quality system is periodically checked and evaluated through the internal quality audits and external audits by ISO certified agencies to provide opportunities for continuous improvement.

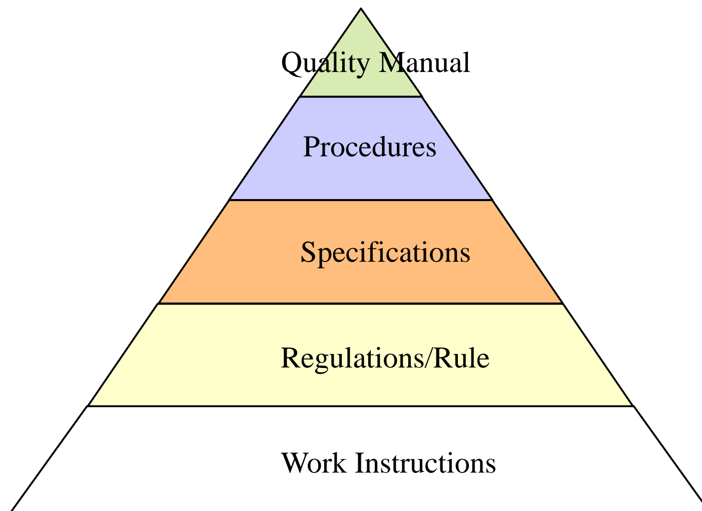


Figure 1-2 Quality Document System

ISSI in USA was certified to ISO 9001:1994 in Sept 1995. With the continuous effort in quality improvement, ISSI achieved the ISO 9001: 2000 standard in July 2002. All ISSI locations passed ISO9001 assessments in 2005 conducted by Underwriters Laboratories (UL), one of the leading international certification bodies, as shown by the certificate issued in Figure 1-3.

ISSI is not only certified to ISO/9001 but also achieved the required quality system level as required by ISO/TS16949 through team effort in the past few years. ISSI has implemented ISO/TS16949 quality system requirements and has successfully passed several automotive customer audits that are leaders in the international automotive industry. All employees are moving forward through continuous improvement.

UNDERWRITERS LABORATORIES INC.

CERTIFICATE OF REGISTRATION

Integrated Silicon Solution, Inc. (ISSI)
1940 Zanker Road, San Jose, CA 95112, USA

Corporate Registration Includes:

Integrated Silicon Solution, Inc. (Shanghai)
No. 12-13, Lane 647, Songtao Road, Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203, China

Integrated Silicon Solution, Inc.
No. 2, Technology Road, V, Hsinchu Science Park, Hsinchu, Taiwan

with an off-site facility located at:
Integrated Silicon Soluton, Inc.
7F, No. 106, Sec. 1, Hsin-Tai 5th Road, Hsi-Chih, Taipei County, Taiwan

Underwriters Laboratories Inc.® (UL) issues this certificate to the Firm named above, after assessing the Firm's quality system and finding it in compliance with

ISO 9001:2000

EN ISO 9001:2000; BS EN ISO 9001:2000; ANSI/ASQ Q9001:2000

for the following scope of registration

3674 (US): Semiconductors and Related Devices

The design of integrated circuits. The management of outsourced integrated circuit production activities. The remote location at 7F, No. 106, Sec. 1, Hsin-Tai 5th Road, Hsi-Chih, Taipei County, Taiwan performs the following primary functions: sales and marketing activities.

Further clarifications regarding the scope of this certificate and the applicability of ISO 9001:2000 requirements may be obtained by consulting the organization.

This quality system registration is included in UL's Directory of Registered Firms and applies to the provision of goods and/or services as specified in the scope of registration from the address(es) shown above. By issuance of this certificate the firm represents that it will maintain its registration in accordance with the applicable requirements. This certificate is not transferable and remains the property of Underwriters Laboratories Inc. ®.

File Number: A12962 Volume: 1
Original Certification Date: March 29, 2004
ISO 9001:2000 Issue Date: March 29, 2004
Revision Date: November 3, 2008
Recertification Date: November 29, 2008
Renewal Date: November 28, 2011

John H. Schmidt
Senior Vice President, Chief Development Officer

Fig. 1-3 ISSI ISO 9001:2000 Certificate

1.4 Quality Systems

ISSI Quality systems have evolved to comply to ISO/TS 16949 compliance. While not all ISSI product are shipped to automotive, the system requirements have been embraced to attain more robust quality processes.

1.4.1 Process Map

The inter-relation ship of ISSI systems is shown in the Fig 1-4.

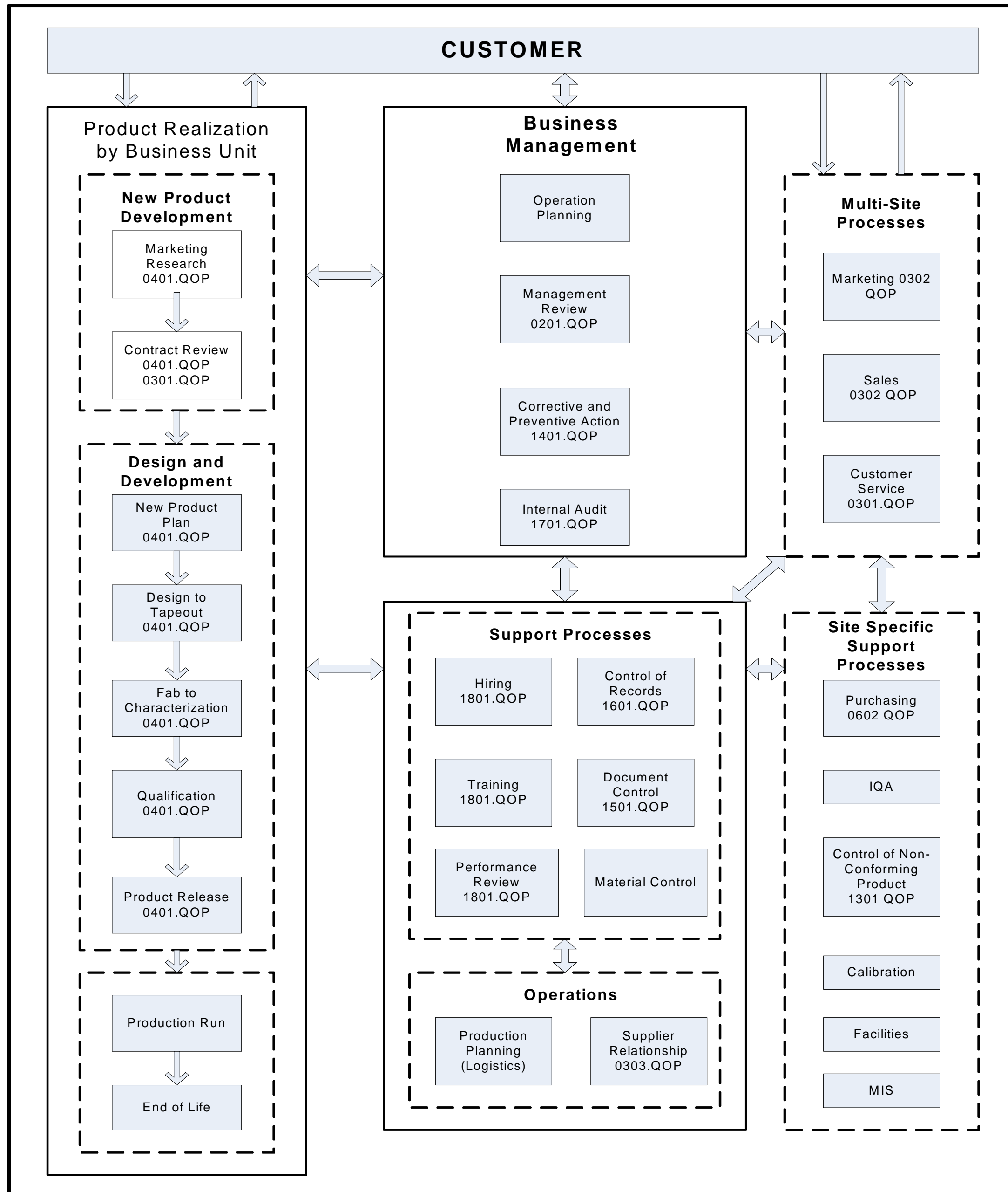


Fig 1-4 Process Map

Process	Sales/ Marketing	Design Engineering	Technology Development	Product Engineering	Assembly Engineering	Reliability Engineering	Testing Engineering	QA	Purchase	Production Control
Product Planning Form	1. Issue Product planning form 2. Prepare Data sheet	1.Resource arrangement 2. Plan/ Schedule	1.Foundry/ Technical selection	1. Resource arrangement 2. Production flow identification	1. Assembly selection 2.Resource survey	1. Reliability survey	1. Soft ware development 2. Wafer sort/ Final test survey		1. cost survey	1. Resource survey 2. Cost analysis
New Project Check List	Kick-off Meeting and project approved									
		1. Review DFMEA/ PFMEA/ Control Plan 2. Design rule check 3. Tape out document 4. Design report 5. CAD check 6. Tape-out approval/ meeting	1. Review mask layer spec 2. review Device cross section 3. WAT spec complete 4. Process flow 5. PPAP review (PFMEA, MSA, Control plan, SPC and production flow)	1.Sample preparing stage a. Prepare Sample b. Mosaid program c. ESD/Latch up sample d.Qualification sample e.Characterization & data review 2. Risk production Stage a. CP1 yield trigger b. CP2 yield trigger c. FT yield trigger d. CP test program release e. FT test program release f. PPK review g. Alphi / Beta site test	1. Marking specifica-tion 2. PPAP review (PFMEA, MSA, Control plan, SPC, Production flow) 3. process stage a. lead frame preparation b. Bonding diagram c. IC marking	1. Burn-in diagram 2. HAST diagram 3. PQR report (Device) 4. PQR report (Package)	1. Test program preparation 2. Characterization program/ report 3. Review Handler/ High Fix/ Load board /change kit 4. Wafer sort program preparation 5. Probe card	Review/ Monitor every process	Follow up wafer out schedule	Handle small volume/ middle volume and mass production
Release Meeting	Release / Start Check meeting									

Figure 1-5 New Project Checklist

1.4.2 Advanced Product Quality Planning

ISSI linked together the requirements of the automotive Advanced Product Quality Planning by setting up a New Project Checklist (NPCL) System. The system is web based and can be accessed by all the team members. In the NPCL system, all the steps and requirements for the life of a product can be documented and tracked. The following processes contribute to the success of the NPCL

1.) Product Planning – Marketing gets the new project approved

2.) New Product Plan – Marketing endorses the project to Design who will work with Marketing, Development and Engineering to put the product plan together

3.) Design and Development – at this stage, Design works with Technology Development for the actual Design of the product taking into consideration customer requirements for the product. One tool used at this stage is the Design FMEA. FMEAs are discussed in the succeeding section.

4.) Process Development – it is at this stage that Design and Technology Development work with Product Engineering and Assembly Engineering and QRA to develop the Production Design and Product Flow. It is also at this point that the requirements for qualifying the product are planned to verify if the actual performance of the product meets the intended characteristics. At this stage, additional tools are identified such as Production flows, Control Plans and Statistical Methods for controlling the characteristics of the product. It is also at this stage that the tool Product Part Approval Process is utilized.

5.) Product Verification – the plans for verifying the conformance of the product to required characteristics is executed

6.) Prototypes – ISSI also builds product prototypes which are a limited quantity of risk builds are produced as needed. During these builds the conditions and controls are the same as actual production. At this point, preliminary Cpks are already computed and studied.

7.) After the successful production of risk builds, then the product is ready for full production and ramp up. Samples for customer qualification have already passed and customers have already given feedback to ISSI on the product performance in their application.

8.) Any problems encountered during the steps of the NPCL requires corrective action and lessons learned are recorded. For problem solving, ISSI uses the 8Discipline (8D) method. Any problems encountered during the life of the product will undergo this process of problem resolution.

The interrelation shown in Figure 1-5 represents the activities and different department's involvement during each phase of Advanced Product Quality Planning.

The major milestones determine the status of each new product including project approval, design development, and release to production. Each of the indicated departments must approve the new product release to production based on defined objectives that include product performance and quality.

1.4.3 Quality Assurance in the Project Approval Stage

Before starting product planning, it is essential to carry out market research activities to ascertain the intended applications and the product quality/reliability demanded by each customer, and also to understand technical trends in the general marketplace, basic specifications, delivery requirements, prices, quality, reliability and other demands on products.

Information on demanded quality and reliability acquired through the above activities, various data obtained in-house from accumulated results and fundamental research on reliability technology are used to set target levels which are appropriate for product applications and operating environments and to formulate development plans.

This information is then compiled into product plans, and design specifications are drawn up based on these product plans and summarized as input for design.

1.4.4 Quality Assurance in the Design Development Stage

1.4.4.1 Product Development and Design

Product design is an extremely important process for ensuring high quality and reliability in semiconductor devices, and it is necessary to implement both built-in quality and built-in reliability.

Product design proceeds according to the design specification. These specifications include design inputs (applicable regulations, customer demands and in-house standards) to ensure that appropriate requirements are considered. Product design goes through the stages of logic/circuit design, layout, mask design, prototype manufacture and evaluation before reaching completion.

1.4.4.2 Design Review

Design review consists of checking whether the design standards are the rules to be followed. Observance of design standards is checked using various simulation tools automatically or manually.

ISSI provides simulation models for each SRAM, DRAM and EEPROM part manufactured. These models are revised as new device and technologies are developed. Models for logic products may be requested; they are developed as needed. Models can be obtained by contacting ISSI FAE department.

In addition, characterization data on each device are performed and retained in ISSI Notes database. These characterization data are available upon request on a case-by-case basis.

1.4.4.3 Product Release

The final stage before a new product is released to manufacturing is Product Release. During the final product release meeting all requirements of the NPCL are reviewed for completeness and the checklist of items for the product released are discussed. When all are supplied of the satisfaction of the team, the documentation is signed off and the product is officially released together with the qualification and characterization data to demonstrate that the product can be manufactured in accordance to requirements.

1.4.4.4 Production Part Approval Process (PPAP)

As part of the NPCL process, the requirements of the PPAP for automotive products are supplied whenever a product is being qualified for automotive applications.
ISSI will supply the Certificate of Design, Construction and Qualification (CoDC) as well as the Part submission Warrant (PSW) together with the various specific requirements by the automotive customer.
ISSI subcontractors (Fab and Assembly) also submit their own PPAP to ISSI for new technologies and processes.

1.4.5 Quality Assurance in the Production Stage

1.4.5.1 Wafer Processing

1) Wafer Process Technology

Since ISSI is one of the IC design leaders in the world, we serve hundreds of customers with different needs and applications. In order to satisfy all customers' needs, we offer the memory and logic products with leading-edge IC process technologies in 90nm, 0.11-micron, 0.15-micron and 0.18-micron generations.

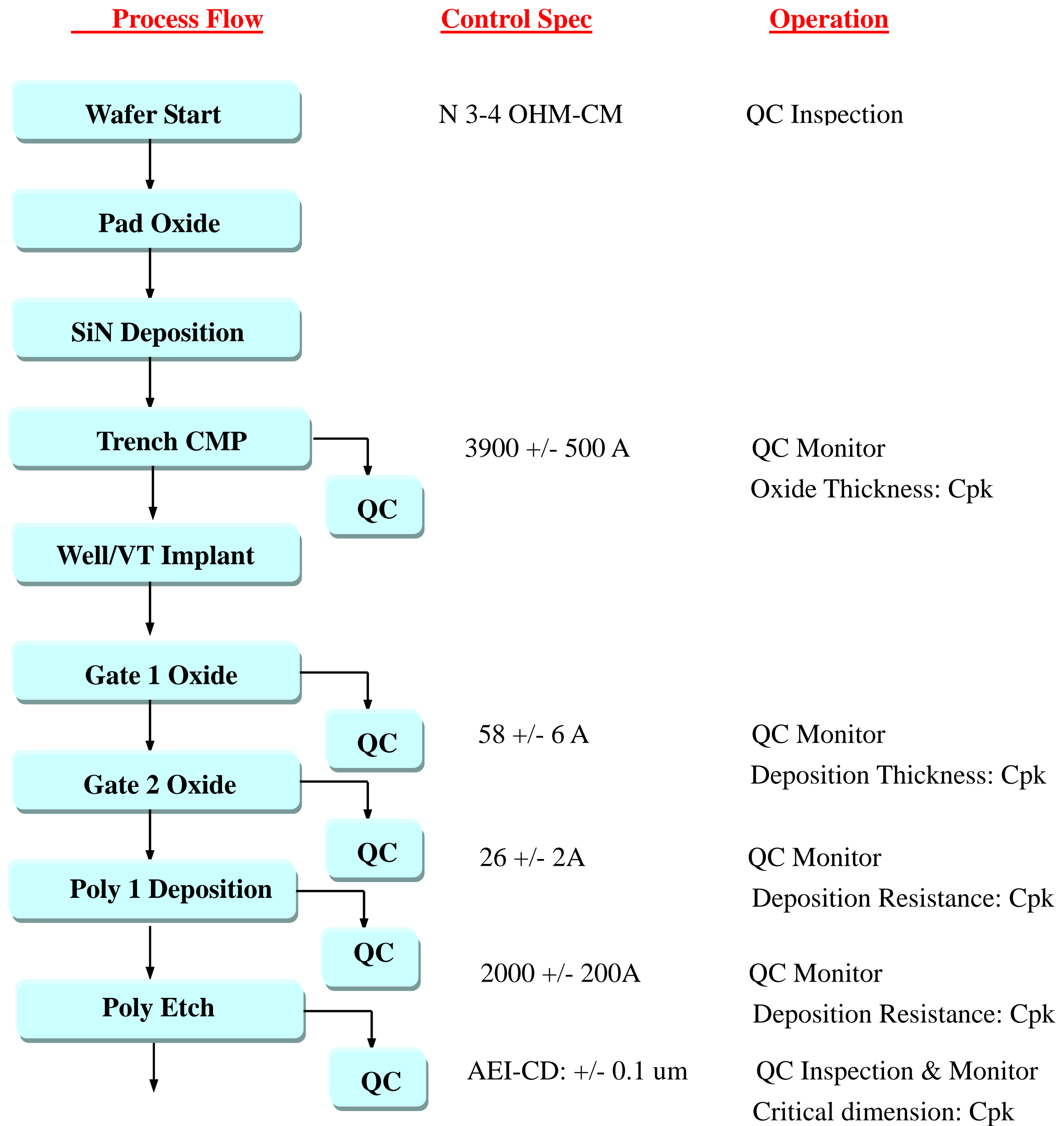
The process technology is developed in accordance with standardized methodologies. Each new technology must pass a rigorous qualification procedure based on typical industry standards before it is released to mass production.

Once in production, every released process is constantly monitored against a predetermined set of standards. The monitor results are then published in the foundry's website and ISSI QA will periodically access the database for evaluation.

Products released to production are monitored at the wafer and package level. Wafer acceptance test (WAT) data by lot indicate key process measurements tested to specified limits. Packaged units are periodically monitored for reliability based on package family and assembly line.

2) Wafer Process Flow and In-line Control

The generic wafer process flow and major control items are shown in Figure 1-6 with SRAM as an example.



To be continued

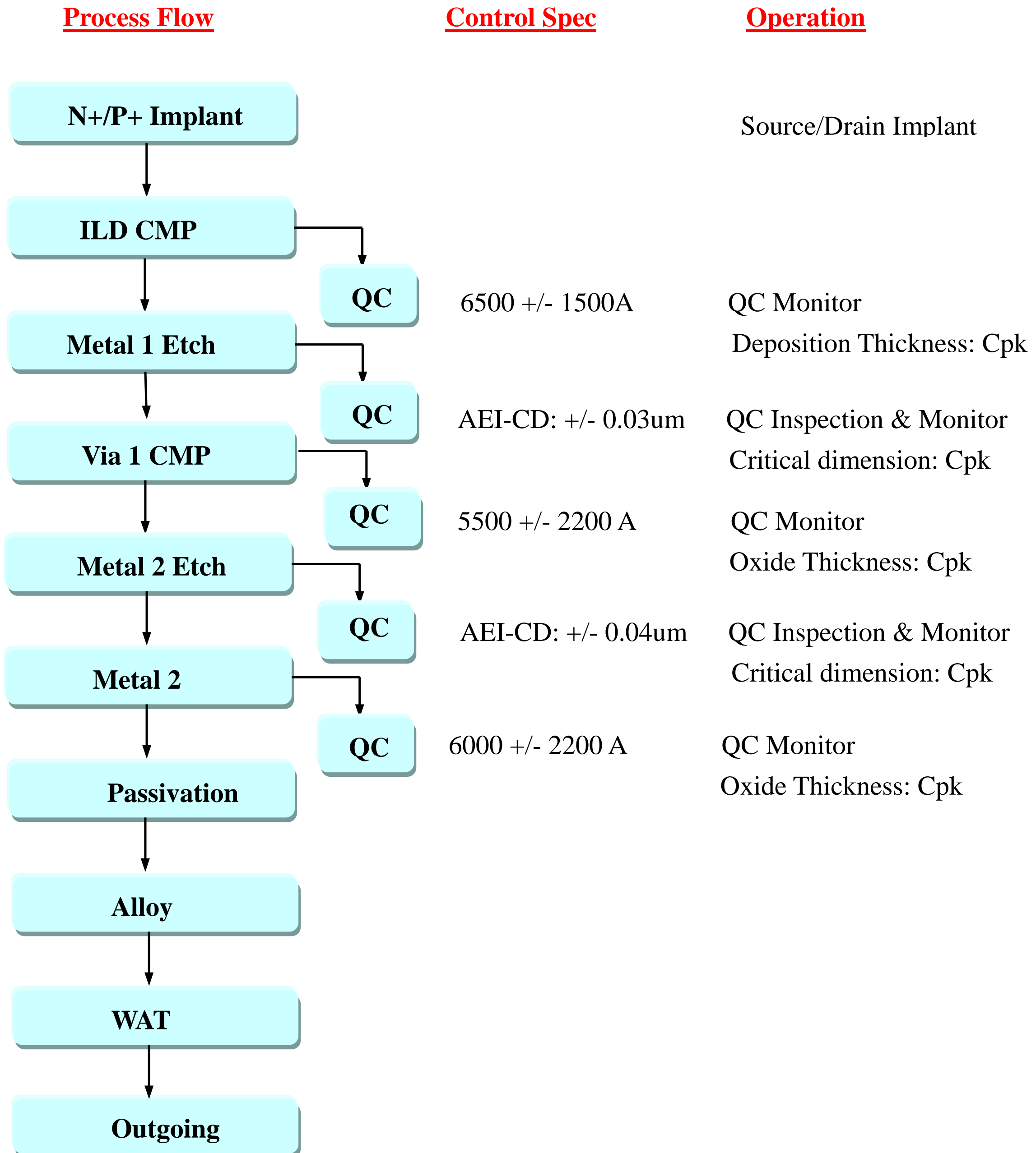


Figure 1-6 Generic SRAM Wafer Process & Control

1.4.5.2 Assembly Process Technology

Our qualified assembly houses offer IC packaging design and fabricate a full array of packaging for ISSI products, with pin counts from 8 to more than 365. Major packaging offers include ball grid array (PBGA, TFBGA), quad flat packages (PQFP, TQFP, LQFP), small outline packages (SOP, TSOP, SOJ), and PLCC. To ensure that they create world-class packages, the major assembly houses are ISO 9000, TS16949 and ISO 14001 certified companies.

The generic assembly process flow and major control item are shown in Figure 1-7.

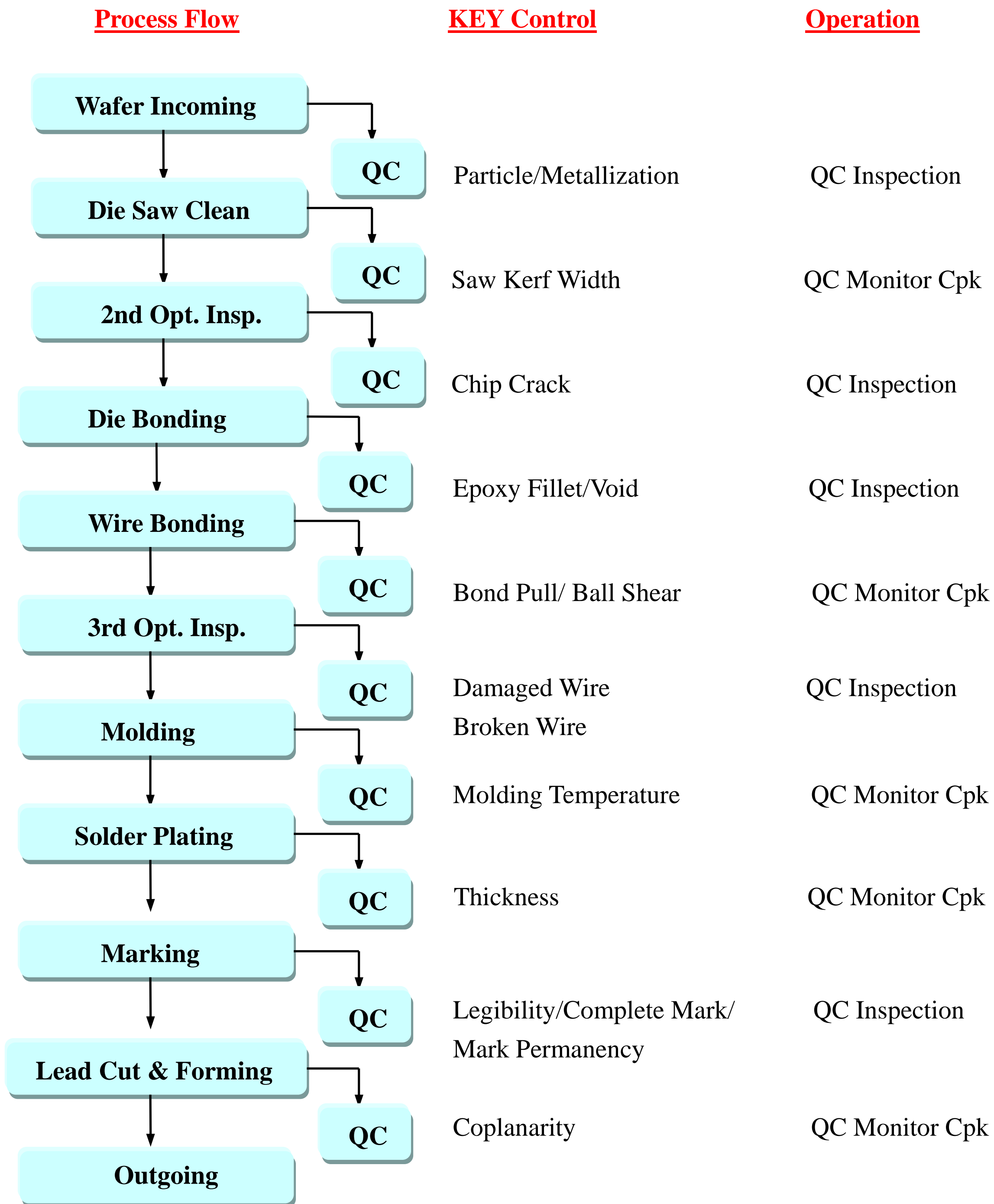


Figure 1-7 Generic Assembly Process & Control

1.4.5.3 Testing

1) Overview

The purpose of testing is to verify the conformance to ISSI specifications and/or customer requirements before the products are delivered to customers. Testing is an inspection process that is needed because the failures have not been eliminated. The failures are usually caused by design errors, materials and process defects, operational environment extremes, and aging effects.

Although testing does not add value to the product, ISSI recognizes it is crucial to recruit skilled engineering expertise to guarantee testing quality. This requires a sizable investment, however, we believe it is a necessity for any company intending to become, or remain as, a leading logic and memory supplier.

Electrical testing consists of three steps: 1) continuity test, 2) DC parametric test, and 3) functional and dynamic test (AC). It is used for verifying IC performance and conformance to ISSI published data sheet so that "bad" parts[1] are not shipped to the customers. The electrical specification limits and conditions are related to the wafer fabrication process parameters and thus to the potential physical defects that might occur.

2) SRAM/DRAM/Logic/EEPROM Product Testing Flow

The Commercial SRAM, DRAM, Logic and EEPROM TEST Flow & Control are shown in Figures 1-8 to 1-11 respectively.

3) Known Good Die Testing Flow

In addition to the package products, ISSI also provides known good die (KGD) business and service to our customers upon request. The generic KGD Test Flow and Control is shown in Figure 1-12.

[1] The unit of measurement for this is typically a parts-per-million (ppm) value for the defective parts shipped to customer.

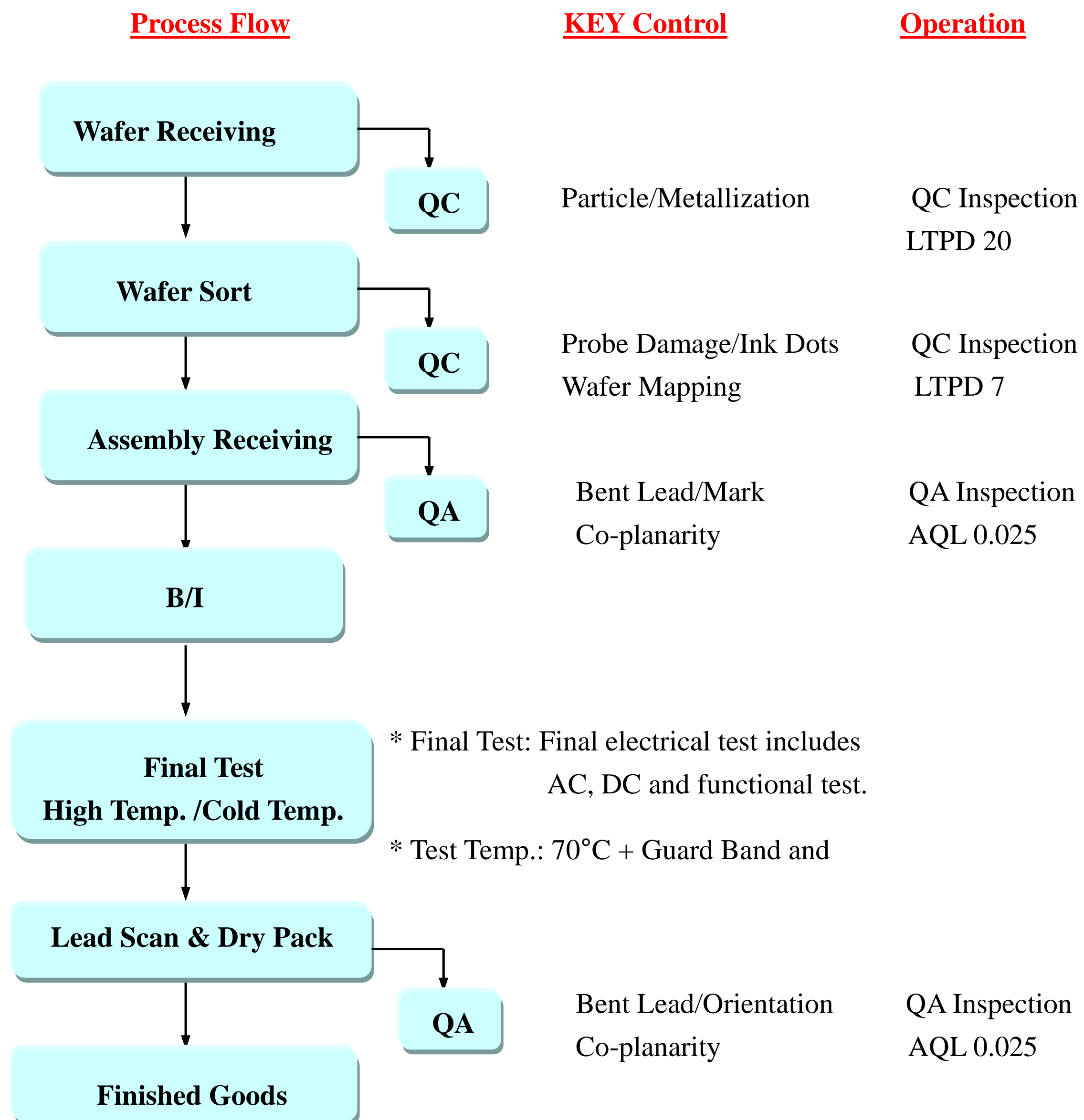


Figure 1-8 Commercial SRAM Test Flow & Control

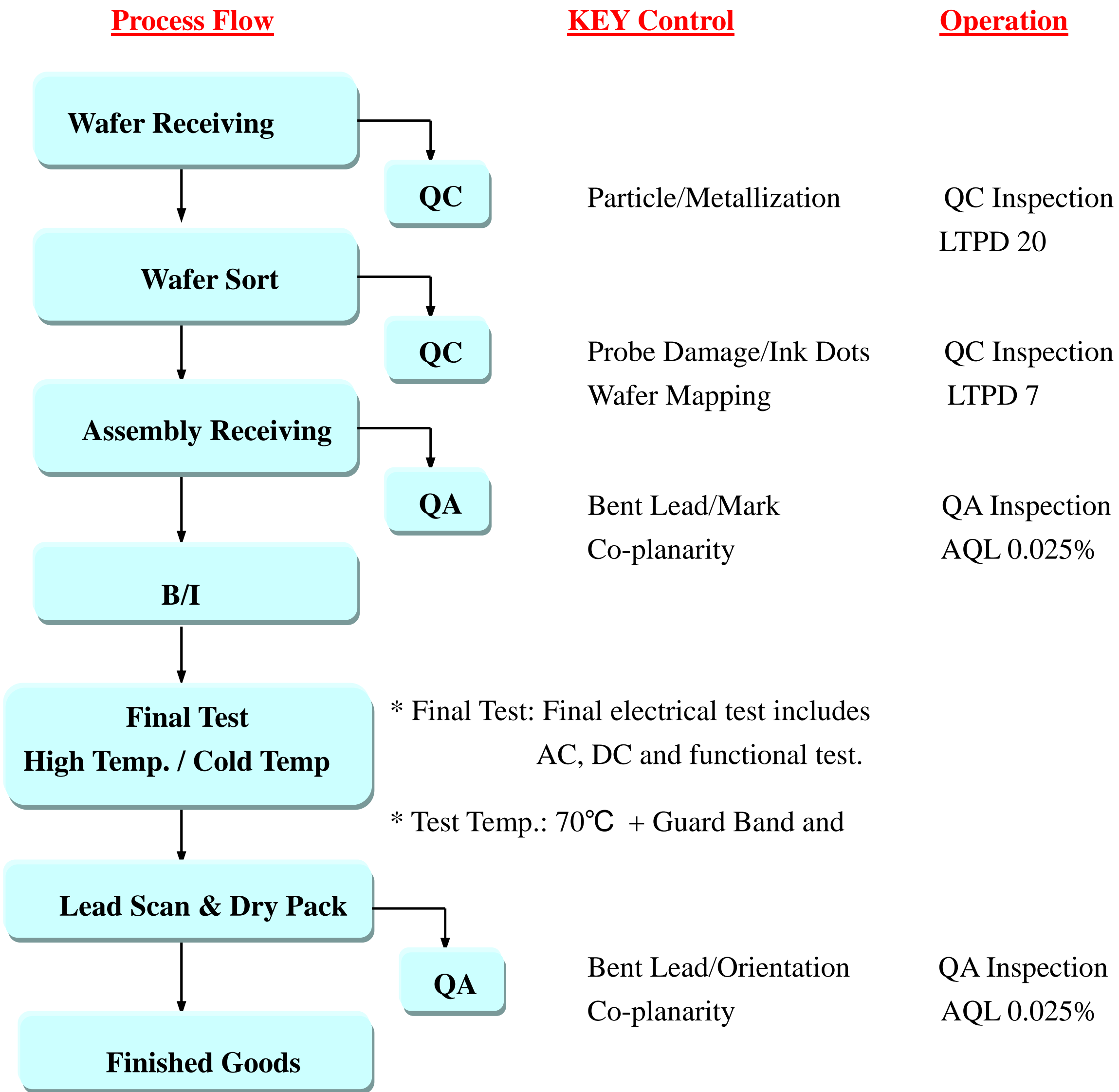


Figure 1-9 Commercial DRAM Test Flow & Control

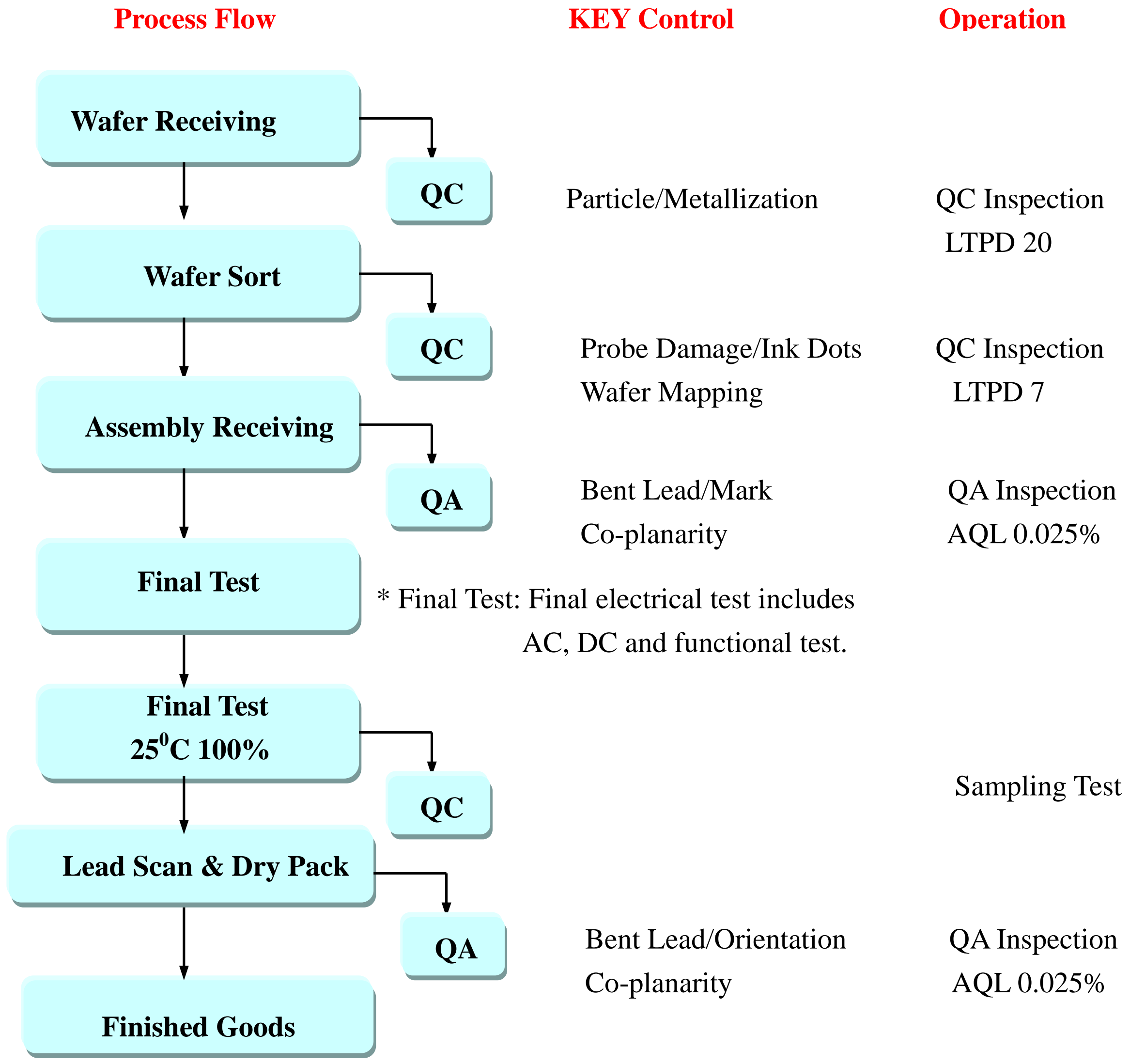


Figure 1-10 Commercial Logic Product Test Flow & Control

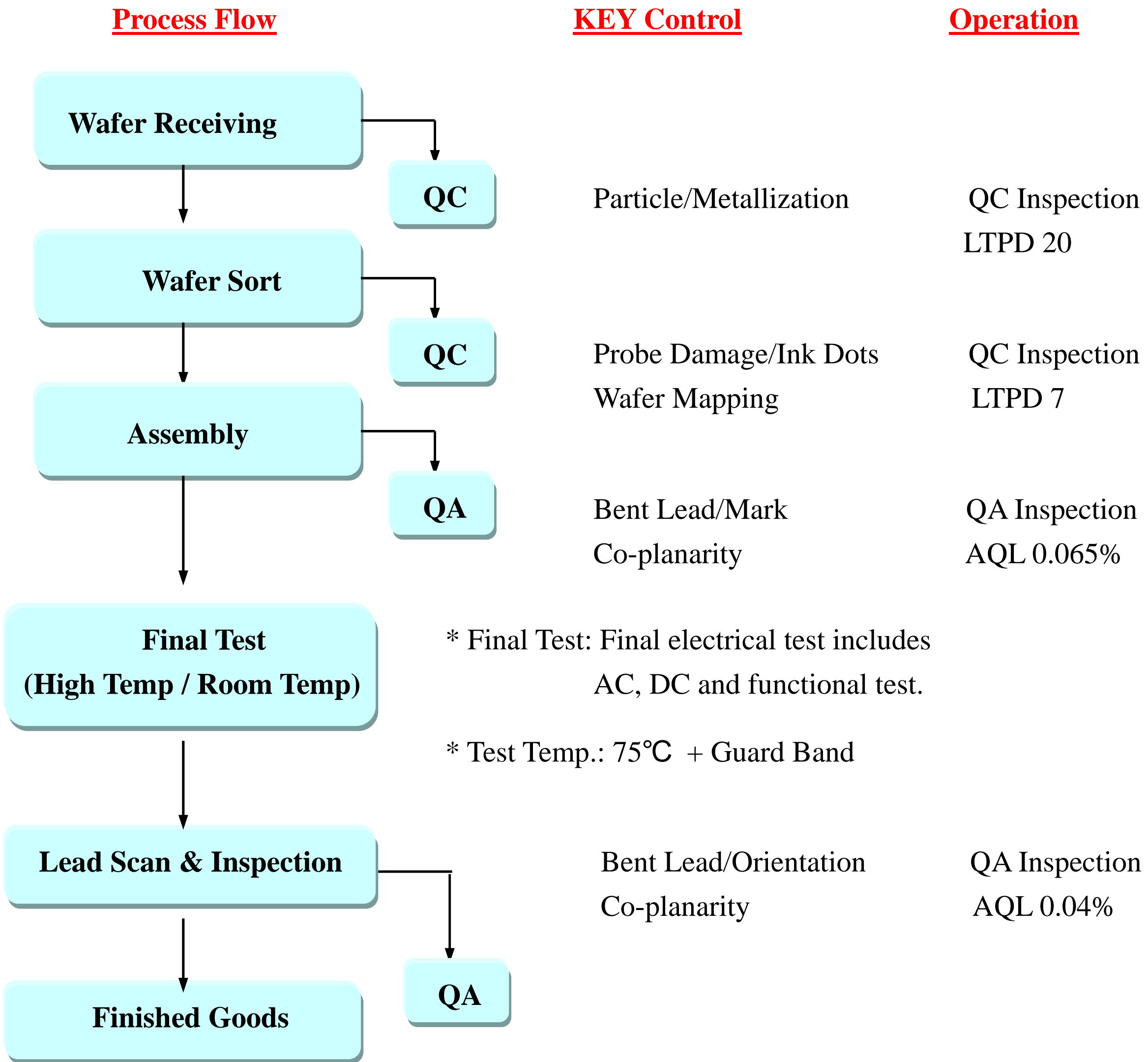


Figure 1-11 Commercial EEPROM Test Flow & Control

1.4.5.4 ISSI offers die only material to customers. These die could be in wafer or in individual die form. Also, the customer can choose an option of tested die without speed testing (Known Tested Die) or die that had gone through burn-in and full testing (Known Good Die)

See Known Good Die flow below:

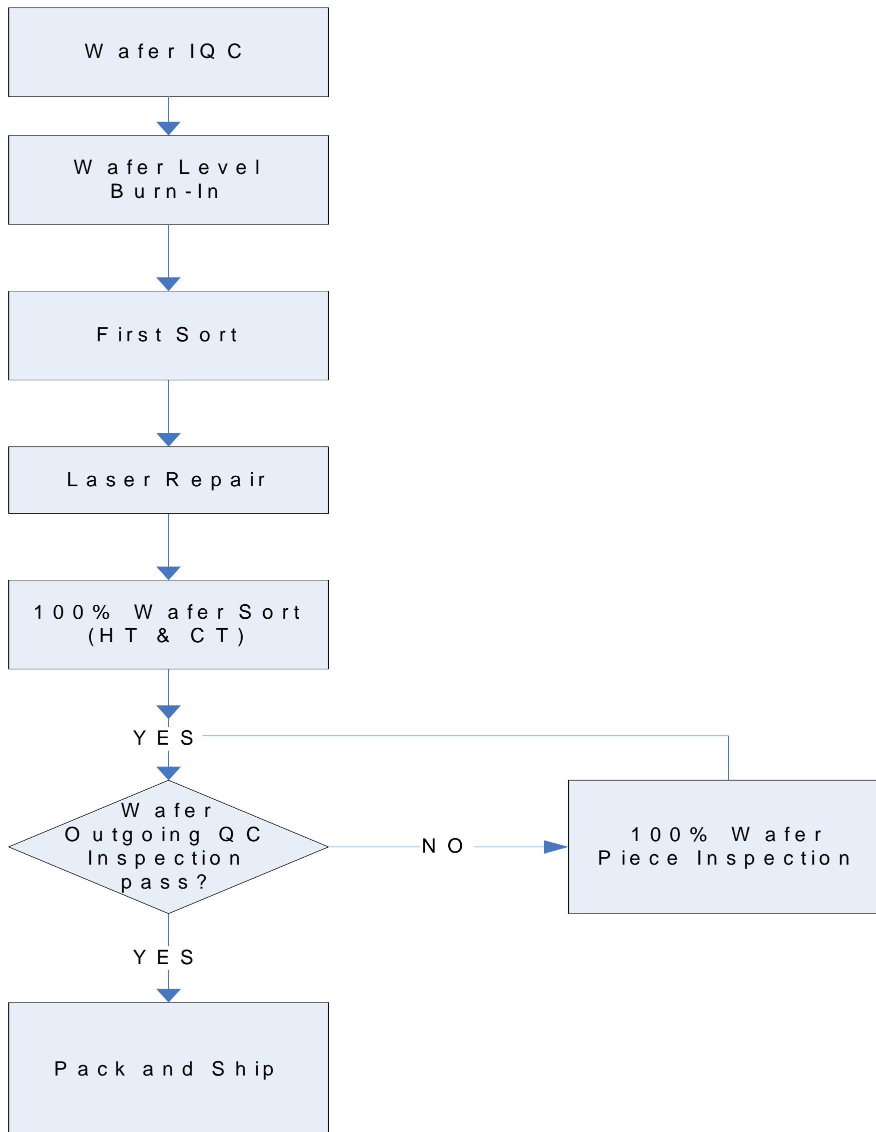


Figure 1-12 Known Good Die Test Flow & Control

4) Monitoring Data for AOQL

ISSI establishes outgoing quality level target, measurement and procedure for continuous improvement.

a) The target of outgoing quality level for all ISSI products is less than 20 ppm. This target is periodically reviewed by management representative to approach the goal of zero defects.
b) All the device types will be measured to establish the outgoing quality level. QC shall issue quality discrepancy report (QDR) for the devices that fall below the targeted quality level and require analysis improvement until the desired quality level is achieved.
c) The average outgoing quality level (AOQL) is sampled from the tested parts at the packing stage in the testing subcontractor, and the sample lots should be included to be tested by each testing subcontractor.

Outgoing quality levels will be published by QRA and distributed to appropriate persons. The monitoring data in the year of 2008 are shown in Table 1-1 to Table 1-4.

For logic products, they are manufactured by order. There are very few devices in stock and the AOQL is not monitored at present.

1.4.6 Quality Assurance of Product Shipping

Checks are carried out to ensure that the quality control established in the development and manufacturing stages is being reliably executed. Shipping inspections are performed to confirm the quality assurance of each lot in order to ensure the quality and reliability of shipped products.

The shipping inspection includes visual check and sampling of electrical characteristics. Visual check consists of checks on lead bending, marking defects, chipping, voids and defects. Electrical characteristics involve DC and AC characteristics as described in (section 1.4.5.3.4.C) “Monitoring Data for AOQL”.

After the final inspection, judgment is made to confirm that the electrical specifications, appearance and packing condition of shipped products satisfy the specifications demanded by customers.

1.5 Change Control

Quite often, changes are made to products or manufacturing process in order to improve quality, reliability and/or productivity.

The feasibility of these changes is judged using sufficient data indicating that the change will not produce any negative effects.

When a change is planned, all related departments review the change and its potential impact. In the case of changes that have a significant effect on product, these results are conveyed in advance to customers to confirm that there is no deteriorated effect at the customer side.

After these judgments are received, if the change is acceptable, instructions are issued and initial control of floating data is performed as necessary for the final check.

The ISSI change list is shown below (Table 1-8) and its system flow is depicted in Figure 1-13.

Item	Lead Time
Die Technology	3 months
Foundry Site	3 months
Wafer Fabrication Process	3 months
Assembly House	3 months
Assembly Process	3 months
Marking	3 months
Data Sheet	3 months
Packing	3 months
Discontinue	6 months

Table 1-8

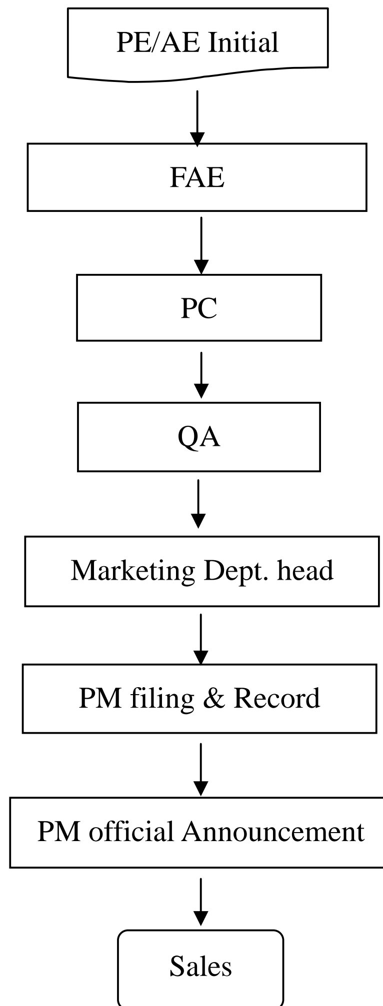


Figure 1-13 ISSI Change System

1.6 Customer Complaint

1.6.1 ISSI RMA Process

Field quality information is an essential factor for improvement of product quality. Equally important are the investigation of field failures and feedback of results to the customers.

When a customer desires to return product, a return material authorization (RMA) form identifying the customer, the product, and the nature of the customer's concern should be completed. There are six types of returned material that ISSI accepts from customers. These are :

1) Administrative:

Customer received wrong parts, wrong quantity, order entry error, duplicate shipment barcode label errors, etc. Shipping discrepancies must be reported within 60 days of shipment.

2) Customer Convenience:

Customer doesn't want the parts even though they are what they ordered and work according to specification.

3) Electrical:

Parts failed to function as specified or did not work in the application.

Electrical RMAs usually require an FA.

4) Failure Analysis:

Customer has requested in depth failure analysis on returned part(s)

5) Stock Rotation:

Product returned from distributors

6) Visual/Mechanical:

Visual inspection failures such as bent leads, coplanarity, tape & reel

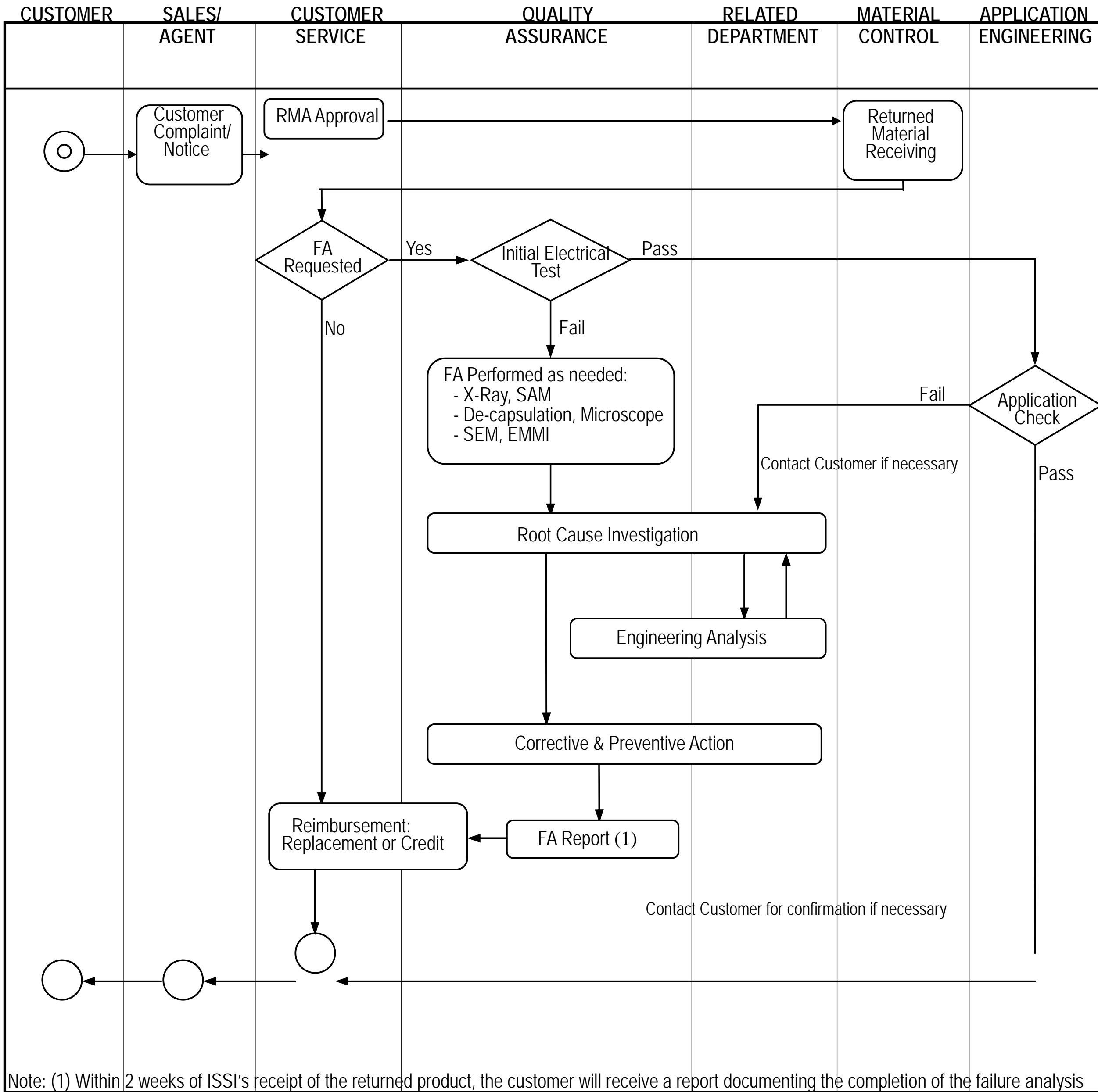
If the RMA involves a quality issue, a FA RMA is requested and the appropriate failure analysis engineer is immediately notified. A customer who needs to receive information on the cause of the failure can request failure analysis to be performed. Within 48 hours of ISSI QRA's receipt of the returned product, a preliminary report will be issued, to verify the customer complaint.

If the product function meets ISSI specifications, the customer will be contacted and the application will be investigated

If, on the other hand, the product proves to be defective, a failure analysis will be done to determine the cause and corrective action will be taken. Within two weeks of ISSI QRA's receipt of the returned product, the customer will receive a final report documenting the completion of the failure analysis and the cause of the failure.

1.6.2 RMA Flow Chart

ISSI has developed procedures and e-RMA system for providing and controlling returns from customers for failure and non-failure issues. See flow as shown in Figure 1-14 for failure issues.



and the cause of failure.

Figure 1-14 RMA Process Flow

1.6.3 2008 RMA Trend Chart

The RMA trend charts in the year of 2008 are shown in Table 1-6 and Table1-7.

1.7 e-CAR

For ISSI's commitment to continuous quality improvement, a corrective action request (CAR) procedure is established according to the ISO 9001:2000 and JEDEC 671 standard. The Corrective Action methodology follows the 8 Discipline process.

1.7.1 Corrective Action

ISSI shall take action to eliminate the cause of non-conformities in order to prevent recurrence. Corrective actions shall be appropriate to the effects of the non-conformities encountered. A documented procedure shall be established to define requirements for

1) reviewing non-conformities (including customer complaints),
2) determining the causes of non-conformities,
3) evaluating the need for action to ensure that non-conformities do not recur,
4) determining and implementing action needed,
5) recording the results of action taken, and
6) reviewing corrective action taken.
7.) verifying that the action taken is effective

1.7.2 Preventive Action

ISSI shall determine action to eliminate the causes of potential non-conformities in order to prevent their occurrence. Preventive actions shall be appropriate to the effects of the potential problems. A documented procedure shall be established to define requirements for

1) determining potential non-conformities and their causes,
2) evaluating the need for action to prevent occurrence of non-conformities,
3) determining and implementing action needed,
4) records of results of action taken, and
5) reviewing the preventive actions taken.

The electronic Corrective Action Request (e-CAR) system was established by ISSI IT and QRA. The e-CAR is used to record and track the most important quality issues including in-house design and operations, customer complaint, and subcontractor's processes. The data is reported to periodic corporate meeting and quarterly management review meeting.

The e-CAR Report_as shown in Figure 1-15 is a listing of the CAR's accumulated year to date. Each individual CAR is accessible electronically on the database. Online CAR can also be searched by date, processor or status as shown in Figure 1-16.

CAR
- 1. CCAR
- 2. ITR
- 3. PAR
- 4. VenCAR
  - 4.1 By Created Date
  - 4.2 Record No
  - 4.3 By Status
  - 4.4 By Processor
  - 4.5 Gate
  - 4.6 By Lot No
  - 4.7 Location
  - 4.8 Need Calim
  - 4.9 Report
- AllDocuments
- Conflicts

New Document

建單號	流程狀態	下一位簽核者
11/11/2008		
10/21/2008		
10/20/2008		
09/28/2008		
09/17/2008		
09/15/2008		
09/10/2008		
09/02/2008		
08/15/2008		
08/11/2008		
07/01/2008		
06/13/2008		
06/11/2008		
05/19/2008		
05/16/2008		
05/14/2008		
05/13/2008		
05/02/2008		
04/23/2008		
04/02/2008		
03/25/2008		
03/17/2008		
03/14/2008		
03/11/2008		
02/29/2008		
02/27/2008		
02/19/2008		
02/13/2008		
01/30/2008		

Figure 1-15 e-CAR Report

CAR New
- 1. CAR
  - 1.1 By Created Dat
  - 1.2 Record No
  - 1.3 By Status
  - 1.4 By Processor
  - 1.5 Gate
  - 1.6 By Lot No
  - 1.7 Location
  - 1.9 Report
- 2. ITR
- 3. PAR
- AllDocuments
- Conflicts

New Document

CAR No.	Cause	Device	Status	End Cus.	Req. Date	Closure Da	Part No.
CAR2007039	N/A	S1001 controll	Cancel (97)	Customer hidden (confidential)	09/28/2007		
CAR2007040	Human error		Close (99)		09/28/2007	12/20/2007	IS24C02-3G
CAR2007041			Close (99)		09/28/2007	12/07/2007	
CAR2007042	poly-1 extrusion	D007	Close (99)		09/28/2007	10/16/2007	IS42S16400
CAR2007043	mixed unit	5104	Close (99)		09/28/2007	12/20/2007	IS24C64A-2
CAR2007044	Micro Crack	D016	Cancel (97)		09/28/2007		IS45S32400
CAR2007045			Cancel (97)		09/28/2007		
CAR2007046			Close (99)		09/28/2007	12/07/2007	
CAR2007047			Close (99)		09/28/2007	12/07/2007	
CAR2007048			Close (99)		09/28/2007	12/07/2007	
CAR2007049	Current datasheets don't be	D023	Close (99)		09/28/2007	10/16/2007	IS42S32800
CAR2007050	parts were mislabeled	8142	Close (99)		09/28/2007	01/10/2008	IS61WV641
CAR2007051	STI particle	8132AM	Close (99)		09/28/2007	10/16/2007	IS61LV1281
CAR2007052	W missing	D008AP	Close (99)		09/28/2007	01/23/2008	IS45S16100
CAR2007053	poly-1 extrusion	D016	Close (99)		09/28/2007	01/08/2008	IS45S32400
CAR2007054	Unknown	8132AM	Close (99)		09/28/2007	10/15/2007	IS61LV1281
CAR2007055	Epoxy fillet overflow	9051BW	Close (99)		09/28/2007	11/26/2007	IS64LP1283
CAR2007056	poly-1 extrusion	F007	Close (99)		09/28/2007	11/22/2007	IS42S16400
CAR2007057			Close (99)		09/28/2007	12/07/2007	
CAR2007058	Human error	9073	Close (99)		09/28/2007	12/20/2007	IS64LPS128
CAR2007059	miss inspection		Close (99)		09/28/2007	01/17/2008	8076/IS62C1
CAR2007060	test fault coverage	D016AP	Close (99)		09/28/2007	11/22/2007	IS45S32400
CAR2007061	The foreign material may b	D017	Close (99)		10/03/2007	11/29/2007	IS45S32200
CAR2007062	Capacity issues on the exi	N/A	Close (99)		10/09/2007	12/04/2007	IS61LPS512
CAR2007063	poly-1 extrusion	D008	Close (99)		10/12/2007	12/04/2007	IS45S16100
CAR2007064	being covered by the coati	9062	Close (99)		10/23/2007	01/07/2008	IS61NLF12
CAR2007065	test fault coverage	9073	Close (99)		10/24/2007	01/18/2008	IS64VF1283
CAR2007066	Application issue_EOS	D008	Cancel (97)		10/31/2007		IS45S16100
CAR2007067	Abnormal laser repair	D016	Close (99)		11/07/2007	01/15/2008	IS45S32400
CAR2007068	Bondability issue	8137	Close (99)		11/07/2007	01/18/2008	IS62WV128
CAR2007069	production flow error	D025	Close (99)		11/07/2007	01/15/2008	IS42S32400
CAR2007070	Human error	D008	Close (99)		11/07/2007	01/19/2008	IS45S16100
CAR2007071	Good	D008	Close (99)		11/20/2007	02/22/2008	IS45S16100
CAR2007072	Good	D008	Close (99)		11/26/2007	01/02/2008	IS45S16100

Disapprove & Return | Cancel CAR | Help

Document Author : Banjie Bautista/Santa Clara/ISSIHQ
Current Server : Emerald/Hsinchu/ICSI
Document Link :

Integrated Silicon Solution Inc.
Corrective Action Request
Status : QA Approver (12)

【Schedule and Assignment】

Serial No. : CAR2008013
Requestor : Jeff Hsiung/Hsinchu/ISSIHQ — **Date** : 03/18/2008 01:29 PM
Product Grade : (•) Automotive ( ) Non-Automotive
D3 Expected Completion Date : 03/19/2008 — **D7 Expected Completion Date** : 03/28/2008
***Assign QA Approver** : Banjie Bautista/Santa Clara/ISSIHQ — ***Assign Marketing Approver** : Ron Kalakuntla/Santa Clara/ISSIHQ
Cycle Time (Containment) : Day, Hour — **QA Personnel** : Angela Lu/Hsinchu/ISSIHQ
Cycle Time (Report) : Day, Hour
Cycle Time (Closure) : Day, Hour — **Closure Date** :

【Basic Information】

Part No : IS45S16100C1-7TLA1 — **Customer** : Flextronics Althofen
Device : D008 — **End Customer** : Philips APM
Lot No : RLH80600X — **RMA #** : 101RMA-000250
Date Code : 0645 — **FA #** : T08-028
Returned Qty : 1 — **Returns Received Date** : 03/10/2008
Non-Conformance : Pixelated Video — **Root Cause** : poly-1 extrusion
Containment Action Reply Date 03/18/2008 — **Complete Report Reply Date** : 03/19/2008
Notify User : TWNMarketing, Marketing, Sales, TWNTechnologyDevelopment, TWNQAEngineers

【Action】

1 :

Description	Foundry will implement the water rinse flow in the production.
Owner	Ben Yeh/Hsinchu/ISSIHQ, NC Chen/Hsinchu/ISSIHQ
Commit Date	10/01/2007
Actual Date	10/01/2007
Extension Date	
Extension Reason	

2 :

Description	
Owner	
Commit Date	

Figure 1-16 e-CAR Example

Chapter 2 Management on Subcontractors

2.1 Task Force

On average, 40% of production cost is due to material procurement; therefore, subcontractor management is extremely important. It follows that a substantial portion of quality problems is related to the subcontractor. Establishment of a partnership is essential in order for both parties to succeed their business. Consequently, the subcontractor is treated as an extension of ISSI production process.

The subcontractor should make a positive contribution to design, production, and cost reduction. Emphasis should be placed on the total material cost, which includes that of price and quality. In order to ensure high quality, ISSI QA is performing on-site process monitoring via a task force unit as shown in Figure 2-1.

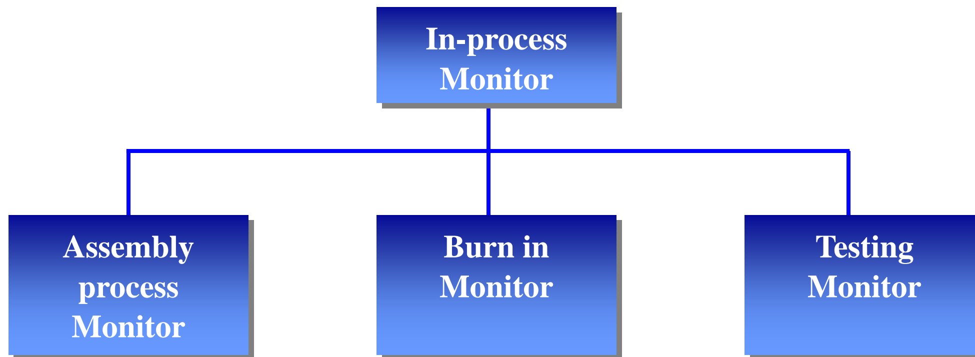


Figure 2-1

2.2 Methodology

Subcontractor management activities include:
1) Subcontractor qualification & Approved Vendor List control
2) Control of bill of material (BOM) and process
3) Package IQC
4) Monthly key process Cpk[1] (> 1.67) report
5) Reliability monitoring (plus de-lamination, die crack, and cratering check)

---

[1] Cpk is an index of process capability. It measures the process stability with respect to the standards over a certain period. To calculate Cpk, it is necessary to calculate another index, Cp, which measures the data bias toward the standard center.

$$C_p = \frac{(\text{upper limit} - \text{lower limit})}{6\sigma} \quad \text{and}$$

$$C_{pk} = \frac{|\text{standard limit closest to the average value - average}|}{3\sigma}$$

where σ is the standard deviation

6) Foundry/ Assembly/ Testing house rating
7) Monthly/ Quarterly meeting with key subcontractors
8) In-process monitor
9) Process control (Man, Machine, Material, Method)
10) Product output (inspect good and reject parts in each stage)
11) ISSI finding and reporting
12) Subcontractor's action and continuous improvement

2.3 Quality Rating

Subcontractor quality ratings provide an objective measurement of a subcontractor's performance. This measurement will lead to a subcontractor review, allocation of business, and identification of the areas for quality improvement.

The vendor quality ratings are based on certain measures and are weighted as follows:

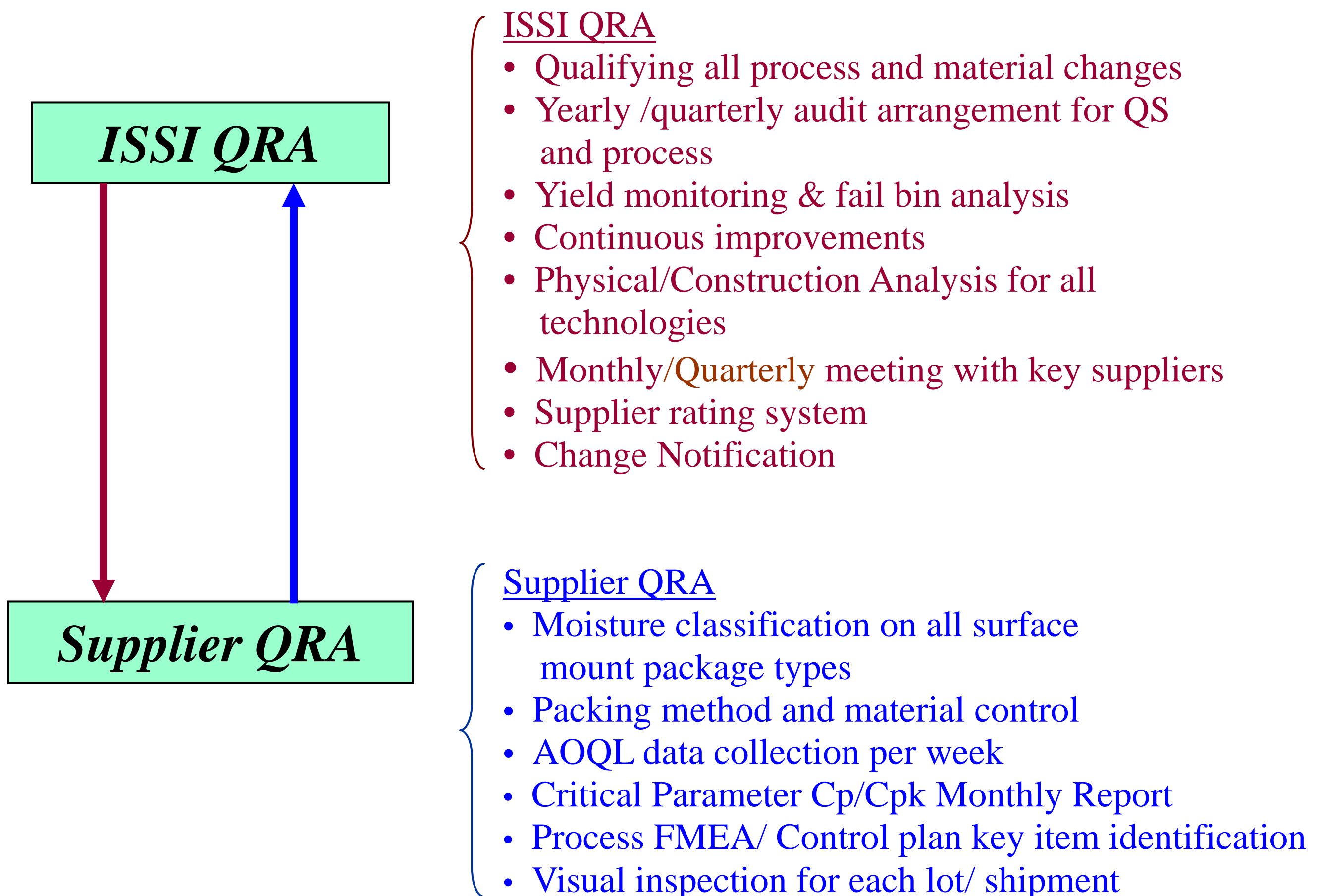
Element	**Point Value**[2]
1. Quality Contribution	**30**
2. Technology	**10**
3. Flexibility/ Service	**20**
4. Cost	**20**
5. Delivery	**20**

[2] Rating result: reduce assembly allocation ration for score less than 70

2.4 Supplier Relationship

Subcontractor relationship is vital to product quality. In ISSI, bi-directional communication/meetings with suppliers are periodically held to review if the supplier performance follows ISSI's requirements closely. The key communication items are defined in the following diagram (Figure 2-2):

Figure 2-2 Supplier Relationship



Chapter 3 Product Reliability

3.1 Reliability Assurance

In the highly competitive market of semiconductors, the requirement for IC component suppliers to deliver very reliable product has resulted in an overall philosophy of quality and reliability assurance. ISSI is committed to ship highly reliable products with reliability results well within specified levels. To ensure the reliability standards, the rules of design, layout and processing are reviewed to cope with the new concepts during the early product development stage. Furthermore, new product /process qualification and production reliability monitoring are performed in order to assure device performance and to accumulate statistical data base information.

3.1.1 Product /Process Qualification

The products used for reliability testing are representative of all device families, package families, foundry locations, and assembly locations. The standards referenced by ISSI are JEDEC Standard 22 and MIL-STD-883, which have been universally used throughout the semiconductor industry.

Reliability is defined as the probability that a semiconductor device will perform its required function under the specified conditions for a stated period of time. The probability of survival prior to time t, $R(t)$, plus the probability of failure, $F(t)$, is always unity. Expressed as a formula:

$$R(t) + F(t) = 1, \quad \text{or} \quad R(t) = 1 - F(t).$$

The probability of survival and failure is derived from the observed results of actual stress tests performed on the devices. High Temperature Operating Life (HTOL) will determine the expected failure rate, $\lambda(t)$, under operating conditions. The other reliability tests, which are described in below, accelerate other expected conditions and contribute further survival /failure rates for both die/process and package.

3.1.1.1 Die/Process Reliability Tests

1) High Temperature Operating Life Test (HTOL)
(Refer to JEDEC 22-B-A108)

High temperature operating life test is performed to accelerate failure mechanisms that are activated by temperature while under bias. This test is used to predict long-term failure rates since acceleration by temperature is understood and the calculation for acceleration factor is well established. Prior to HTOL, all test samples are screened to standard electrical tests at low temperature and high temperature with prior burn-in.

Dynamic operating conditions are applied to most cases and the test circuit is depending on the specific device. The typical stress voltage is 1.1 times of normal operating voltage. Unless otherwise specified, the stress temperature is maintained at 125 °C. Devices are tested at prescribed time-points. Failure rates are calculated in terms of FITs (failures in time). Each FIT represents one failure in 10^9 device-hours.

2) Infant Mortality (IM)

Infant mortality testing determines the early failure rate of a specific product and process. The test conditions are basically the same as the high temperature operating life test with an increased sample size to ensure an accurate failure rate. The test temperatures can be set between 125 °C to 150 °C, depending on product type and the test environment. The typical stress voltage is at least 1.2 times of normal operating voltage. The failure rate data is used to determine a product burn-in strategy for each product and provide information for process improvement.

3) Electrostatic Discharge (ESD)
(Refer to MIL-STD-883C, 3015; JEDEC 22-A114, A115 & ESD-STM 5.3.1-1999)

Electrostatic discharge sensitivity (ESD) tests are designed to measure the sensitivity of each device with respect to electrostatic discharges that may occur during device handling. Various test methods have been devised to analyze ESD. Currently, ISSI evaluate ESD using the following test methods. The human body model (HBM) is in accordance with the standard specified by MIL-STD-883C and JEDEC 22-A114 while machine model (MM) is by MIL-STD-883C/JEDEC 22-A115 and the charge device model (CDM) is by ESD–STM 5.3.1-1999.

The human body model is based on a high-voltage pulse (positive and negative) of longer duration, simulating discharge through human contact. The machine model is based on a high-current short duration pulse to simulate a device coming in contact with a charged surface. The charge device model is based on the phenomenon where the semiconductor device itself carries a charge or where the charge induced to the device from charged object near the device is discharged. It reproduces the discharge mechanism in the form closest to the discharge phenomenon occurring in the field.

4) Latch-up
(Refer to JEDEC standard No. 78)

The latch-up test is designed specifically for CMOS processed devices to detect parasitic bipolar circuits that, when activated, may short power and ground nodes. Test conditions are significantly worse than normal operation variations to provide a margin for safe operation. Presently, ISSI evaluates latch-up based on JEDEC standard No. 78. For JEDEC standard, current (positive and negative) is injected into individual

input/output pins in steps while the power supply current is monitored. The current into the test pin must rise to a minimum of 100 mA without a latch-up condition. .

5) Soft Error Rate
(Refer to JEDEC Standard 89)

Semiconductor memory defects that can be recovered by rewriting the data are called soft errors. In addition to being caused by the power supply line and ground line noise, soft error are also caused by α-rays emitted from the trace amounts of uranium, thorium and other radioactive substances contained in the package or wiring materials.

There are two methods for evaluating soft errors: system tests which consist of actually operating large number of samples, and accelerated tests using a α-ray source.

When evaluating the absolute soft error value it is necessary to conduct system tests. However, system tests require many samples and long times (typically, 1000 samples and 1000 hours or more).

In contrast, accelerated tests allow evaluation in a short time, but have the problem that it is difficult to accurately obtain accelerated characteristics for a market environment.

Soft error rates are expressed in FIT units:
1 FIT = 1 Failure/10^9 Device-hours

6) Endurance Cycling
(Refer to MIL-STD-883 1033, JEDEC 22 A117)

The test is used to evaluate the quality of the tunnel oxide of EEPROM products. Continued program-erase operation can cause charge trapping or even breakdown in the tunnel oxide, resulting in threshold shift and eventually failure of a cell to retain data. The test requires 1000k cycles at room temperature or 100K at high temperature. Large electrical field changes between the gate and drain of the memory cell can also cause damage of the oxide layer.

7) Data retention
(Refer to JEDEC 22 A117)

The test is to measure the stability of electron in the floating gate of EEPROM products. Devices are exposed to high temperature, typically, 150 ^{o}C, which causes acceleration of charge loss or gain, resulting in shifting of threshold voltage. No bias is needed for this test. Charge trapping or defect in tunnel oxide and other dielectric, mobile ion contamination may contribute to the degrading of data retention performance.

3.1.1.2 Package Reliability Tests

1) Highly Accelerated Stress Test (HAST)
(Refer to JEDEC 22-B-A110)

The highly accelerated stress test provides constant multiple stress conditions including temperature, humidity, pressure and voltage bias. It is performed for the purpose of evaluating the reliability of non-hermetic packaged devices operating in the humid environments. The multiple stress conditions accelerate the penetration of moisture through the package mold compound or along the interface between the external protective materials and the metallic conductors passing through package. When moisture reaches the die surface, the applied potential establishes an electrolytic condition that corrodes aluminum conductors and affects DC parameters of the device. Presence of contaminants on the die surface such as chlorine greatly accelerates the corrosion process. Additionally, excessive phosphorus in the passivation will react under these conditions.

2) Unbiased Autoclave (Pressure Cooker Test)
(Refer to JEDEC 22-B-A102)

The autoclave test is performed to evaluate the moisture resistance of non-hermetic packaged units. Devices are subject to pressure, humidity, and elevated temperature to accelerate the penetration of moisture through the molding compound or along the interface of the device pins and molding compound. Expected failure mechanisms include mobile ionic contamination, leakage along the die surface, or metal corrosion caused by reactive agents present on the die surface. The autoclave test is performed in a pressure chamber capable of maintaining temperature and pressure. Steam is introduced into the chamber until saturation, then the chamber is sealed and the temperature is elevated to 121 °C, corresponding to a pressure of 33.3 psi (2 atm). This condition is maintained for the duration of the test. Upon completion of the specified time, the devices are cooled, dried and electrically tested. .

3) Temperature Cycling Test (TCT)
(Refer to JEDEC 22-B-A104)

Temperature cycling test accelerates the effects that changes in the temperature will cause damage between different components within the specific die and packaging system due to different thermal expansion coefficients. Typical examples of damage caused by this test include package cracking, cracking or cratering of the die, passivation or metal de-lamination, and more subtle damage resulting impaired electrical performance. During testing devices are inserted into a chamber where the interior is cycled between specified temperatures and held at each temperature for a minimum of ten minutes. Temperature extremes depend on the condition selected in the test method. The total stress corresponds to the number of cycles completed at the specified temperature.

4) Preconditioning Test (Moisture Sensitivity)
(Refer to JEDEC 22-B-A112, A113)

Surface mount packages may be damaged during the solder reflow process when moisture in the package expands rapidly. Two test methods are utilized to determine which packages may be sensitive and what level of sensitivity exists. JEDEC test method A112 classifies devices into three groups, 1) not sensitive, 2) moisture sensitive, and 3) extremely moisture sensitive. JEDEC test method A113 establishes the reliability of devices exposed to a specified preconditioning process at various moisture levels by subjecting preconditioned devices to HAST, PCT and TCT. The test result determines whether dry packing is necessary to ensure the reliability of the product after the assembly process.

5) Solderability
(Refer to JEDEC 22-B-B102)

The solderability test is used to determine the ability of package leads wetted by solder. This test verifies that the method of lead treatment to facilitate solderability is satisfactory and will allow successful solder connection to designated surface. The test is accomplished by immersing leads in flux then dipping the leads into molten solder of 245°C ± 5°C. No less than 95% coverage of the dipped area should be shown on each lead.

6) Mark Permanency
(Refer to JEDEC 22-B-B107)

The mark permanency test subjects package marking to solvents and cleaning solution commonly used for removing solder flux on circuit boards to ensure the marking will not become illegible. Devices and a brush are immersed into one of three specified solvents for one minute, and then removed. The devices are then brushed ten strokes. This process is repeated three times for each group of solvents and devices. After they are rinsed and dried, the devices are examined for legibility according to specified criteria.

7) Lead Integrity
(Refer to JEDEC 22-B-B105)

The lead integrity test provides tests for determining the integrity of devices leads, welds and seals. Devices are subject to various stresses including tension, bending fatigue and torque appropriate to the type of lead. Devices are then examined under optical microscope to determine any evidence of breakage, loosening or motion between the terminal and device body.

8) Bond Pull and Shear
(Refer to MIL-STD-883C, Method 2011.7)

The purpose of these tests is to measure bond strength, evaluate bond strength/bond strength distributions or determine compliance with specified bond strength requirements of the applicable acquisition document.

3.1.2 Qualification Test Method and Acceptance Criteria

The summary shown in Table 3-1 gives brief descriptions of the various reliability tests. Not all of the tests listed are performed on each product and other tests can be performed when appropriate.

	Test item	Applied with	Test method	Test condition	Sample #	Acc No	Comments
1	High Temp. Operating Life (HTOL)	All ISSI products.	JEDEC 22 A108 MIL-STD-883 1005	T=125°C, Apply Voltage >=1.1Vcc, Dynamic	77 105 132	0 1 2	Acceptable number is upon sample size. For Memory: Target failure rate < 50 FITs at 60% CL after 1 Khrs. (Base on Ea=0.7eV) For Logic: Target failure rate < 100 FITs at 60% CL after 500 hrs. (Base on Ea=0.7eV)
2	Electrostatic Discharge (ESD)	All ISSI products.	MIL-STD-883 3015 ESD-STM 5.3.1 - 1999	Human Body Model (HBM) R=1.5kohm, C=100pF. Machine Model (MM) R=0 ohm, C=200pF.	5 HBM 5 MM 5 CDM	0 0 0	5 samples for each test mode (Vic+/, Voss+/, pin to pin). HBM >/= +/-2000V. MM >/= +/-200V. CDM >/=+/-500V (>=0.35um) ; +-250V (>=0.15um)
3	Latch-up	All ISSI products.	JEDEC STD No. 78	Current trigger	5	0	5 samples for each test mode (I trigger) > +/- 100 mA
4	Infant Mortality	All ISSI products.		T=125°C, Vcc applied upon device types, Dynamic.	1140	1	Target failure rate < 100 FITs after 96 hrs at 60% CL.
5	Highly Accelerated Stress Test (HAST)	All ISSI products.	JEDEC 22 A110	T=130°C, 85%RH, 33.3 psi, Apply Voltage=1.1VCC 100 hrs	1). 45 2). 77	1). 0 2). 1	Use LTPD 5%
6	Autoclave (Pressure Cooker, PCT)	All pkg types	JEDEC 22 A102-A	T=121°C, 100%RH, 15psi 168 hrs	1). 45 2). 77	1). 0 2). 1	Use LTPD 5%
7	Temperature Cycling	All pkg types	JEDEC 22-B A104 MIL-STD-883 1010	T=-65°C to 150°C, dwell time=10min, Temperature transition time =15 min 250 cycles	1). 45 2). 77	1). 0 2). 1	Use LTPD 5%
8	Pre-condition ing	All pkg types	JEDEC 22 A113 (ref.)	Bake 24hrs @+125°C, moisture soak (level 3: 192 hrs@30°C/60%RH), reflow solder IR @ For non Pb-free: 240°C+5/-0°C, 3X. flux for 10sec, and For Pb-free: 260°C +5/-0°C, 3X flux for 10sec.	77	1	Use LTPD 5%. The parts, passed level 3 test, will be used to do HAST, T/C, PCT. Level 1 & 2 are optional.
9	Physical Dimensions	All pkg types	JEDEC 22 B100 MIL-STD-883 2016		5	0	Use LTPD 50%

	Test item	Applied with	Test method	Test condition	Sample #	Acc No	Comments
10	Solderability	All pkg (ink marking) except BGA (Laser Marking)	JEDEC 22 B102 MIL-STD-883 2003	Pre-condition $T=93^oC+3/-5^oC$, For non Pb-free $T=245^oC+/-5^oC$, and For Pb-free $T=260^oC+/-5^oC$, Dwell time = 5+/-0.5sec, uncovered surface	5	0	Use LTPD 50%
11	Lead Fatigue	All pkg types (except BGA)	JEDEC 22 B105-A MIL-STD-883 2004	1) 2 oz for SOJ and TSOP, 8 oz for other Pkg 2) for bending arc = 90 +/-5 degree 3) 2 cycles for TSOP, 3 cycles for other Pkg	5	0	Use LTPD 50%
12	Mark Permanency	All pkg (ink marking) except BGA (Laser Marking)	JEDEC 22 B107 MIL-STD-883 2015		5	0	Use LTPD 50%
13	Wire Bond Strength	Option to all pkgs	MIL-STD-883 2011		5	0	1.0 mil =>4 grms. 1.2&1.25 mil =>5 grms. 1.3 mil =>6 grms.
14	Die Bond Strength	Option to all pkgs	MIL-STD-883 2011		5	0	Bond shear strength not less than 30 gram.
15	Scanning Acoustic (SAM) Microscope Inspection	For new assembly process, package	Criteria based on new assembly process and package specification	1) Die surface 2) Interface of die and die attach material 3) Interface of lead frame pad and mold	5	0	Before IR-Reflow, 0% delamination on die surface and <10% at the lead finger area. After IR-Reflow, 0% on die surface and <20% at lead finger area.
16	Co-planarity	Only for SMD pkg	JEDEC 22 B108	Measured accuracies within +/- 10% of specified deviation	5	0	Failure specification. Deviation=3 mil.
17	Soft Error	Only for DRAM product	MIL-STD-883 1032	Am-241, test patterns: checker board and reverse checkerboard at room temp.	5	< 1K FITs	Use LTPD 50%. Target failure rate < 1000 FITs/Mbit at 60% CL.

Table 3-1 Qualification Test Method and Acceptance Criteria

	Qualification Test	Test Method	Test Conditions	Samp. Size	Rej. No.	Lots Req.	Comments
1	Endurance Cycling	MIL-STD-883 1033	Program/erase with 00, FF patterns at room temp. 100kcycles required.	77/130	0/1	3	Use LTPD=3. Target failure rate <1%. Cycles = 1000K.
2	Data Retention	JEDEC 22 A117	T=150°C No bias.	77/130	0/1	3	Use LTPD=3. Use the parts passed the endurance cycling test. Target failure rate <1% after 1khrs baking.

Table 3-1-1 Qualification Test Method and Acceptance Criteria
(Nonvolatile memory portion)

The qualification for automotive application should follow the requirements of AEC-Q100. The test items of reliability qualification for automotive are shown as following:

Test Item	Reference Doc.	Test Method	Sample size / lot	Accept	Notes
HTOL (high temp operating life)	AEC-Q100#B1	JESD22A108B	132 X 3 lots	0 fails	Grade 1 : Ta=125C, 1000 hrs.Vcc max operating for both DC /AC parameter F/T check before and after at low, and high temp.
ELFR (early life failure rate)	AEC-Q100-008	JESD22A108B	800X 3lots	0 fails	Grade 1 : Ta=125C, 48 hrs.Vcc max operating for both DC /AC parameter F/T check before and after at low, and high temp.
HTSL (high temp storage life)	AEC-Q100#A6	JESD22A103B	45 X 1 lots	0 fails	Grade 2 : 125C, 1000 hrs. F/T check before and after at high temp

Test Item		Reference Doc.	Test Method	Sample size / lot	Accept Criteria	Notes
ESD	*HBM*	AEC-Q100-002	JESD22A114B	3 device for each steps	2 kV	F/T check before and after at high temp (IV curve check for every 500V and F/T check for every 1kV step)
	MM	AEC-Q100-003	JESD22A115 A	3 device for each steps	200 V	F/T check before and after at high temp (IV curve check for every 50V and F/T check for every 100V step)
	CDM	AEC-Q100-011	JESD22C101	3 device for each steps	750 V	F/T check before and after at high temp (IV curve check for every 100V and F/T check for every 100V step)
Latch-up		AEC-Q100-004	JESD78	6 X 1 lot	100mA 1.5XmaxV	F/T check before and after at high temp (Icc variation check for initial and F/T check for final confirm)
Gate Leakage		AEC-Q100-006	AEC-Q100-006	6 X 1 lot	+/-400 V	F/T check before and after at room temp

Table 3-1-2 Automotive Qualification Test Method and Acceptance Criteria (device portion)

Test Item	Reference Doc.	Test Method	Sample size / lot	Accept	Notes
Preconditioning	AEC-Q100#A1	JESD22A113D	231 X 3lots	0 fails	Prior to TCT, PCT, THB F/T check before and after at room temp Delam. on die surface is acceptable if can pass subsequent tests.
TCT (temp cycling)	AEC-Q100#A4	JESD22A104B	77 X 3 lots	0 fails	Grade 2 : -50C~150C, 500 cycles. F/T check before and after at high temp Decap procedure on 5 units/ 1 lot after test completed, minimum wire bond pull strength (> 3 grams) on 2 corner bonds per corner and 1 mid-bond per side
PCT (autoclave or	AEC-Q100#A3	JESD22A102C	77 X 3 lots	0 fails	121C/15psig/96 hrs F/T check before and after at room temp
THB (temp humidity bias or HAST)	AEC-Q100#A2	JESD22A101B JESD22A110B	77 X 3 lots	0 fails	THB: 85C/85%RH/1000 hrs with bias or HAST: 130C/85%RH/96 hrs with bias F/T check before and after at high temp

Table 3-1-3 Automotive Qualification Test Method and Acceptance Criteria (package portion)

3.1.3 Semiconductor Device Failure Region

Figure 3-1 shows the time-dependent change in the semiconductor device failure rate. Discussions on failure rate change in time often classify the failure rate into three types of early, random and wear-out failure regions (the so-called "bathtub" curve). However, there is no clear definition for determining the boundary between these regions.

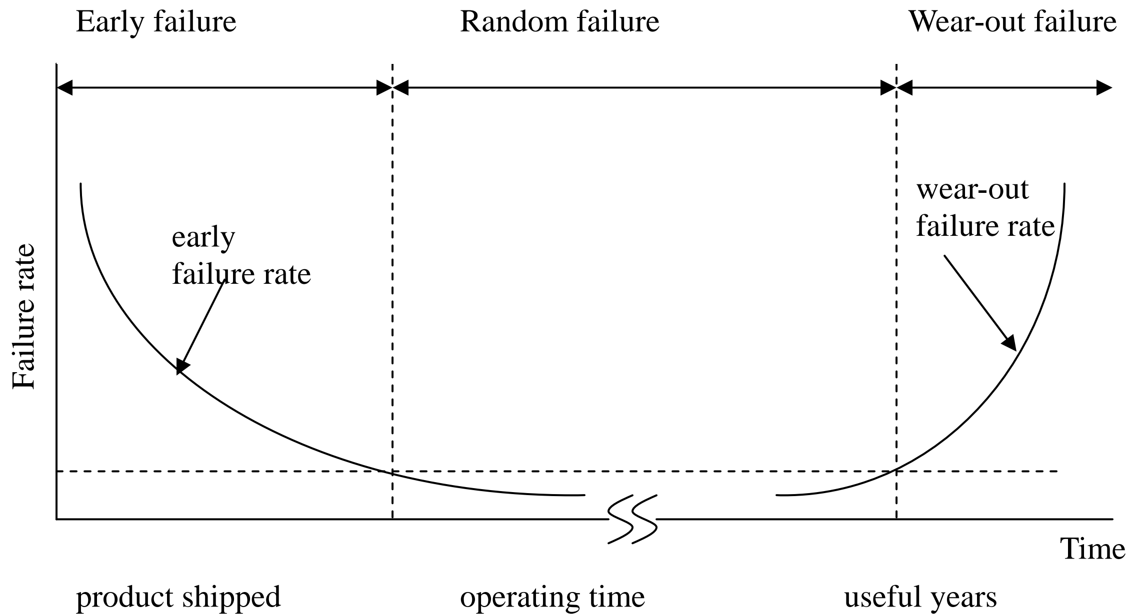


Figure 3-1 Time-Dependent Changes in Semiconductor Device Failure Rate

3.1.3.1 Early Failures

The failure rate in the early failure period is called the early failure rate (EFR), and exhibits a shape where the failure rate decreases over time. The vast majority of semiconductor device's initial defects belong to those built into devices during wafer processing.

While most of these defects will be eliminated in the final sorting process, a certain percentage of devices with relatively insignificant defects may not have failed and may be shipped as passing products. These types of devices are inherently defective from the start and apt to fail when stress (voltage, temperature, etc) is applied for a relatively short period, and exhibit a high failure rate in a short time within the customer's mounting process. However, these inherently defective devices fail and are eliminated over time, so the rate at which early failures occur decreases.

This property of semiconductor devices where the failure rate decreases over time can be used to perform screening known as "burn-in" where stress is applied for a short time in the stage before shipping to eliminate devices containing early defects. Products screened

by burn-in not only improve the early failure rate in the market, but also make it possible to maintain high quality over a long period as long as these products do not enter the wear-out failure region.

3.1.3.2 Random Failures

When devices containing early defects have been eliminated to a certain degree, the early failure rate becomes extremely small, and the failure rate exhibits a constant level over time. In this state, the failure distribution is close to an exponential distribution, and this is called the random failure period.

The device failure rate is normally at a level that can be ignored for the most part. Most of the failures are due to devices containing relatively insignificant early defects (dust or crystal defects) that fail after a long time or random failures such as the memory soft error by alpha particles and other high-energy radioactive rays.

3.1.3.3 Wear-out Failures

Wear-out failures are failures rooted in the durability of the materials comprising semiconductor devices and the transistors, metal lines, oxide films and other elements. In this region, the failure rate increases with time until ultimately all the devices fail or suffer characteristic defects.

The main wear-out failure mechanisms for semiconductor devices are as follows:
1) Time-dependent dielectric breakdown (TDDB)
2) Hot carrier-induced characteristics fluctuation
3) Electromigration

Semiconductor device life is defined as the time at which the cumulative failure rate for the wear-out failure mode reaches the prescribed value, and is often determined by the reliability of each element comprising the device during the process development stage. These evaluation results are incorporated into design rules in the form of allowable stress limits to suppress wear-out failures in the product stage and ensure long-term reliability.

3.1.4 Failure Rate Calculation

Two functions are often used in the evaluation of reliability: probability density function (pdf) of failure $f(t)$ and failure rate $\lambda(t)$.

$f(t)$ denotes the probability of a device failing in the time interval dt at time t. It is related to the Cumulative Distribution Function (CDF), $F(t)$, as $f(t) = dF(t)/dt$.

On the other hand, failure rate $\lambda(t)$ is defined as the instantaneous failure rate of devices having survived to time t. Using the concept of conditional probability, P(B|A) = P(B and A both occur)/P(A), it can be derived that $\lambda(t)$ equals $f(t)/R(t)$ as shown below.

$$\text{instantaneous failure probability} = \frac{\text{fail in next } \Delta t}{\text{survive to } t} = \frac{F(t+\Delta t) - F(t)}{R(t)}$$

$$\text{instantaneous failure rate} = \lambda(t) = \frac{\lim_{\Delta t \to 0}[\frac{F(t+\Delta t) - F(t)}{\Delta t}]}{R(t)} = \frac{f(t)}{R(t)}$$

In the following discussion, the failure rate calculation is described according to the stages of product lifespan.

3.1.4.1 Methods for Estimating the Early Failure Rate

Weibull distribution is applied to approximate the CDF of early failure period; it can exhibit a shape where the failure rate decreases over time.

Weibull distribution is characterized by two important parameters, scale factor (α) and shape factor (β). They are defined as:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right] = 1 - R(t)$$

where t : life cycle or life time (EFR duration to failure)
α : scale factor or characteristic function
β : shape factor or shape parameter

Rearranging the equation, one obtains:

$$1 - F(t) = \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right]$$

$$\ln[1 - F(t)] = -\left(\frac{t}{\alpha}\right)^{\beta}$$

$$\ln[-\ln(1 - F(t)] = \beta \ln t - \beta \ln \alpha$$

When plotted in ln [- ln (1 – $F(t)$)] against t on log scale (Fig. 3-2) , the data should approximately fall on a straight regression line. Scale factor α can be obtained from the intercept of the straight line; it is constant for a fixed test condition. Shape factor β is the slope of the straight line and its value is less than one for early failure period.

Using the relationships that $f(t) = dF(t)/dt$ and $\lambda(t) = f(t)/R(t)$, one can derive the failure rate as:

$$\lambda(t) = \frac{\beta t^{\beta-1}}{\alpha^{\beta}}$$

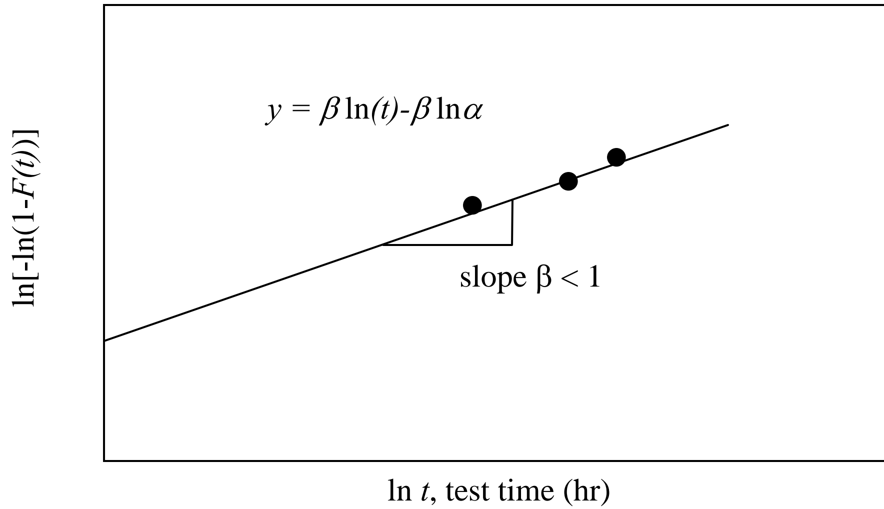


Figure 3-2

3.1.4.2 Methods for Estimating the Useful Life Failure Rate

When devices containing early defects have been eliminated to a certain degree, the initial failure rate becomes extremely small, and the failure rate exhibits a gradually declining curve over time. The failure rate at this period is obtained by dividing the number of failures observed by the device hours, usually expressed as failures per billion device hours (FITs). This is called point estimate because it is obtained from observation on a portion (sample) of the population of devices. In order to determine the unknown population parameter from known sample statistics, it is necessary to make use of specific probability distribution. The chi-square distribution (χ^2) that relates observed and expected frequencies of an event is frequently used. The relationship between failure rate at stress conditions and the chi-square distribution is shown in the following formula:

$$\lambda_{stress} = \frac{\chi^2(\alpha, n)}{2t}$$

where:

λ_{stress} = failure rate at stress conditions
χ^2 = chi-square function
α = (100 - confidence level) /100
n = degree of freedom = $2r + 2$
r = number of failures
t = device hours

The chi-square values for α equal to 60% and 90% at r between 0 and 12 are shown in Table 3-2.

Chi-Square Distribution Function			
60% Confidence Level		**90% Confidence Level**	
No. Fails	χ^2 Quantity	No. Fails	χ^2 Quantity
0	1.833	0	4.605
1	4.045	1	7.779
2	6.211	2	10.645
3	8.351	3	13.362
4	10.473	4	15.987
5	12.584	5	18.549
6	14.685	6	21.064
7	16.780	7	23.542
8	18.868	8	25.989
9	20.951	9	28.412
10	23.031	10	30.813
11	25.106	11	33.196
12	27.179	12	35.563

Table 3-2

Since all the reliability tests are performed under accelerated stress condition, it is important to evaluate the acceleration factor of different stresses.

1) Thermal Acceleration Factor

Acceleration factor for thermal stress is calculated using the Arrhenius equation:

$$AF_t = e^{[\frac{E_a}{k}(\frac{1}{273+T_{use}} - \frac{1}{273+T_{stress}})]}$$

where:
- AF_t = thermal acceleration factor
- E_a = activation energy in electron Volts (eV)[1],
- k = Boltzmann's constant 8.62 x 10^{-5} eV / °K
- T_{use} = junction temperature at normal use condition in °C
- T_{stress} = the stress temperature in °C

2) Voltage Acceleration Factor

High electrical field can cause physical damage in the oxide layers. The acceleration factor due to voltage stress is a function of both the stress voltage, V_{stress}, and the wafer process. AF_V can be derived from Eyring model as:

$$AF_v = e^{\gamma(V_{stress} - V_{use})}$$

where:
- AF_V = voltage acceleration factor
- γ = constant in 1/V
- V_{stress} = stress voltage
- V_{use} = use voltage

3) Humidity Acceleration Factor

For humidity acceleration test, the acceleration factor can be estimated by

$$AF_h = \left(\frac{RH_{stress}}{RH_{use}}\right)^m$$

[1] The activation energy is defined as the excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur. Examples are the energy needed by the molecule to take part in a chemical reaction, by an electron to reach the conduction band in a semiconductor, or by a lattice defect to move to a neighboring site. (Ref. *Van Nostrand's Scientific Encyclopedia*) ISSI's failure rate calculations are based on acceleration from high temperature where thermal activation energy, Ea, is typically identified in JEDEC Standard.

where : RH_{stress} = relative humidity in stress
RH_{use} = relative humidity in use (typical value 17.6%)
m = experimentally determined (typical value m = 3)

If temperature is included in the humidity test, both temperature and humidity acceleration factor need to be considered.

In THB test (Temp/Humidity/Bias), the voltage acceleration factor must be added. The junction heating effect can reduce the relative humidity. For example, a 5°C junction heating effect by bias can reduce the RH from 85% to 73%.

4) Temp Cycling Acceleration Factor

The acceleration factor can be estimated by

$$AF_{tc} = \left(\frac{T_{\max,stress} - T_{\min,stress}}{T_{\max,use} - T_{\min,use}} \right)^n$$

where : $T_{max,\ stress}$ = high temp in cycling stress
$T_{min,\ stress}$ = low temp in cycling stress
$T_{max,\ use}$ = high temp in field application, usually 70°C
$T_{min,\ use}$ = low temp in field application, usually 0°C
n = experimentally determined, usually n = 5

5) MTTF at Use Conditions

The mean-time-to-failure (MTTF) is defined as the average time-to-failure (or expected time-to-failure) for a population of devices, when operating its required function under the specified conditions for a stated period of time. It can be expressed by:

$$\text{MTTF} = \int_0^\infty tf(t)dt$$

The overall relationship of $F(t)$, $R(t)$, $f(t)$, $\lambda(t)$ and MTTF can be depicted as below (Fig. 3-3) :

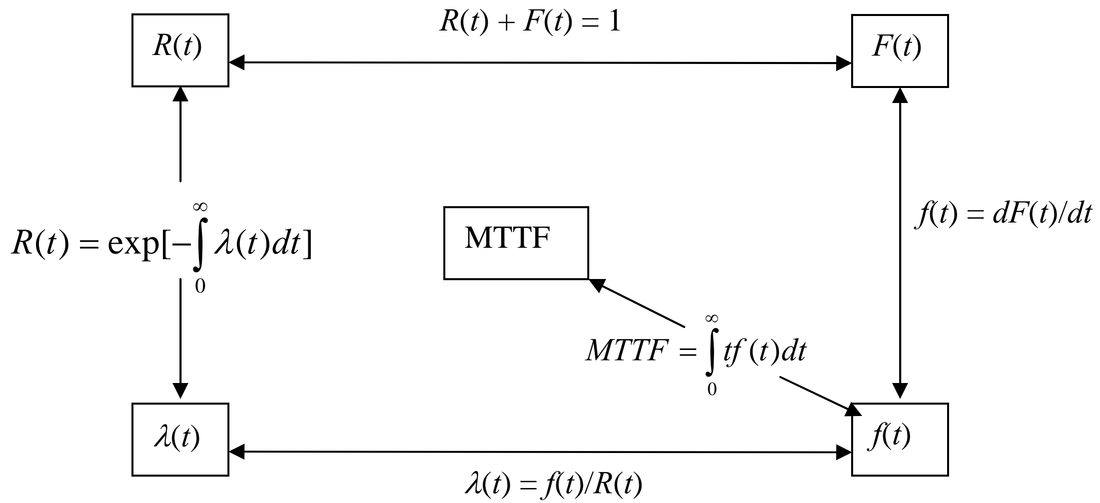


Figure 3-3

For the case of constant failure rate ($\lambda(t)$ = constant), $R(t) = \exp(-\lambda t)$, $F(t) = 1 - \exp(-\lambda t)$ and $f(t) = dF(t)/dt = \lambda \exp(-\lambda t)$

$$\text{MTTF} = \int_0^\infty tf(t)dt = \int_0^\infty t\lambda \exp(-\lambda t)dt = \frac{1}{\lambda_{use}}$$

where the point estimate of the failure rate at use conditions is calculated as:

$$\lambda_{use} = \frac{\lambda_{stress}}{AF_t \times AF_v}$$

3.1.5 Philosophy of Reliability Monitoring

In order to guarantee the high standard of reliability for each product family, a reliability monitoring methodology linked with MTR (electronic- Manufacturing Trouble Report) system is executed. By monitoring the data of post burn-in yield, RAE department will determine if sampling burn-in is needed for any specified lots. To screen out any potential failure parts, it is necessary to do 100% re-burn-in for the whole mother lot if the sampling burn in result is substandard. The reliability monitoring process flow is shown in Figure 3-4.

ISSI Memory Product Process Monitor Plan

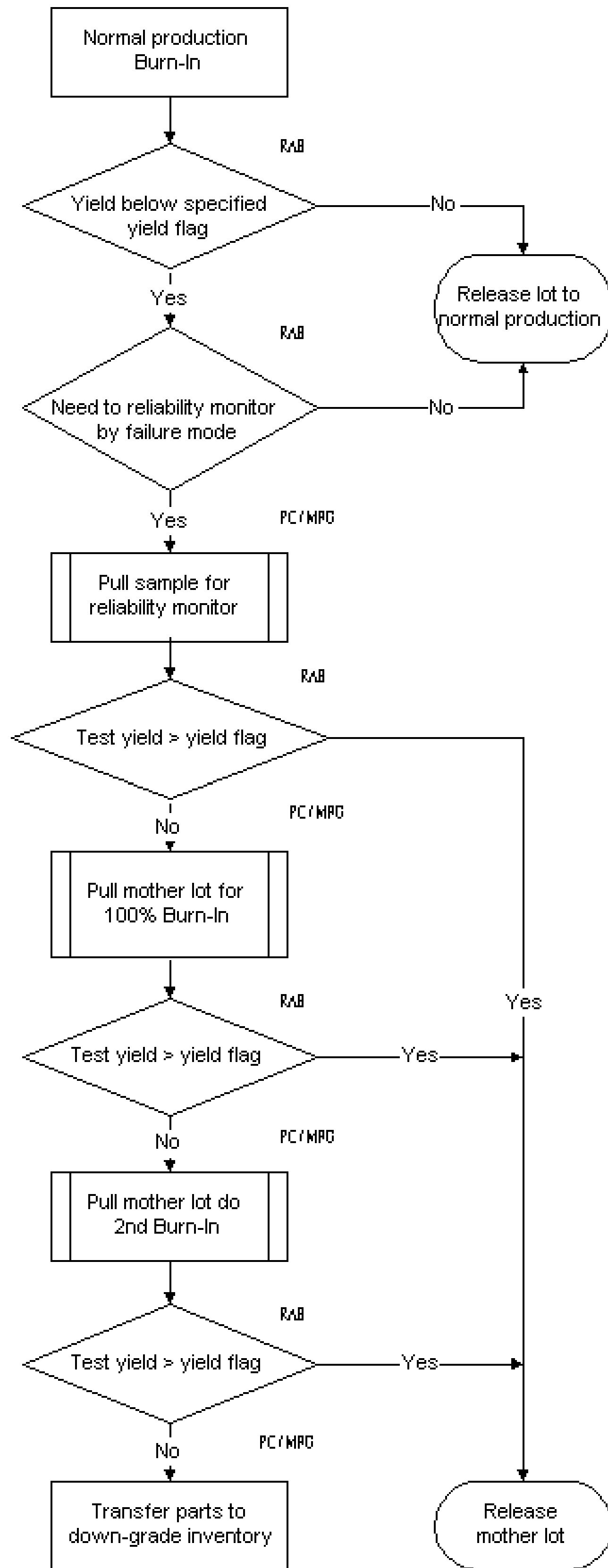


Figure 3-4

3.1.6 Reliability Test Equipment List

The reliability test equipment utilized throughout ISSI's device measurement laboratory and approved subcontractors are shown in Table 3-3.

Figure 3-5 Signality Burn-in Oven, for HTOL test

Figure 3-6 HIRAYAMA Pressure Oven, for HAST test

Figure 3-7 HIRAYAMA Pressure Oven, for PCT test

Figure 3-8 HITACHI Cycling Oven, for TCT test

Figure 3-9 ISUZU High Temp Oven, for HTS test

Figure 3-10 HITACHI Humidity Oven, for THS test

Table 3-3

Category	Item	Application	Application Site
Visual	Stereo Microscope	For visual inspection of wafer and package parts	In-house lab
	Scanning Electron Microscope (SEM)	Inspect surface or cross section of a device at high magnification	In-house lab
	Acoustic Microscope (CSAM)	For visual inspection delamination in package	In-house lab
	Optical Microscope	For visual inspection both wafer and package parts	In-house lab
	X-ray	To inspect the bonding wire of encapsulated devices	In-house lab
Electrical Test	Keytek ESD & Latch-up Test system	To test ESD and Latch-up, both JEDEC and EIAJ modes available	Currently in subcontractor
	Curve Tracer	To measure parameters	In-house lab
	Parameter Tester	To measure parameters	In-house lab
	Oscilloscope	To test timing and functionalities	In-house lab
	Bench testers (GII, Adventest -Tester, EPRO-142,etc.)	To test parametric and functional characteristics.	In-house lab
	MOSAID Tester	To test functionalities and parameters	In-house lab
Stress Test	Temperature Probe System	To probe the device at high temperature.	In-house lab
	HTOL Oven	To do high-temperature operating life test	In-house lab
	HAST Test System	To do highly accelerative stress test	In-house lab
	Temperature Cycling System	To do temperature cycling test (-65 ℃ to 150 ℃)	In-house lab
	Bake Oven	To do baking and data retention test.	In-house lab
	Temp.& Humid. Storage Chamber	To do high temp and humidity soak test.	In-house lab
	PCT Test System	To do pressure cooker test.	In-house lab
	IR-reflow chamber	To do preconditioning test.	In-house lab
	Other Package Related Tests	To quality the leads, marking, etc.	In-house lab

3.2 Device Related Test Data

(All test data are shown in Table 1-8 to Table 1-17 in the appendices except the data of Soft Error Rate)

3.2.1 High Temperature Operating Life Test

Condition : Dynamic operation, T = 125 °C
Duration : Up to 1000 hrs, failed device were counted at 72, 500 and 1000hrs
Failures : When a device fails to pass production test program
Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed.

3.2.2 Infant Mortality Test

Condition : Dynamic operation, T=125 °C
Duration : Up to 96 hrs, failed device were counted at 8, 16, 24 and 96 hrs
Failures : When a device fails to pass production test program
Calculation : Both temperature and voltage acceleration factors are considered for the failure rate calculation; Poisson probability distribution with confidence level = 60% is assumed

3.2.3 Electrostatic Discharge (ESD) and Latch-up Tests

ISSI currently performs three types of ESD tests :

1) The Human Body model (HBM), according to MIL-STD-883, method 3015 and JEDEC standard No.A114,
2) The Machine model (MM), according to JEDEC standard No.A115,
3) The Charge Device model (CDM), according to JEDEC standard No.22-C101.

During the tests, the applied voltage is increased in steps until reaching the maximum passing voltage.

The test sequence for ESD is listed as following:

1) Zap all pins (+/-) respectively to V_{DD} and Vss pins.
2) Zap all pins (+/-) respectively to all other pins.
3) Zap all V_{DD} pins (+/-) respectively to all Vss pins.

Latch-up test: In accordance with JEDEC standard No.78, the currents are injected into the input, output and I/O pins, and I_{cc} is monitored to see whether latch-up has occurred.

The test sequence of latch-up is listed as following:

1) Current trigger to all pins (+/-) respectively with all input pins biased during V_{DD} power is applied.
2) Voltage trigger to all V_{DD} pins respectively with all input pins biased during V_{DD} power is applied.

3.2.4 Soft Error Rate
(JEDEC Standard 89)

Source : Americium 241, with half life = 432.7 ± 0.5 years
Alpha particle activity: 4.948K Bq[2]
Alpha particle flux density: 4.53×10^5 / cm^2-hour
Acceleration factor: source α-intensity / package α-intensity.
Example: for molding compound with an emission of 0.001/cm^2-hr, the acceleration factor = 4.53×10^8,
Test condition: After de-capsulation, the radioactive source was directly placed over the die surface. Both the source and die were covered to avoid ambient light; Pattern is written into the cell and data are continuously read out.

Device	Memory Size	Product #	Process	Lot	Die Size (mil)	Geometric factor[3]	Vcc (V)	FITs
A006AT	4M	IC61LV25616-10T	TSMC-0.25um 3P2M	WA459800P1	371x166	0.308	3.3	15.1
D002AV	16M	IC42S16100-7T	VIS-0.18 um 4P2M	P1100184E	105x181	0.0398	3.3	0
E007AU1	16M	IC41C16100-35K	UMC-0.21 4PDM	IA3490CLD	110x232	0.3876	5.0	0
E007AU2	16M	IC41LV16100-50T	UMC-0.21 4PDM	I99160QLD	110x232	0.8432	3.3	0
E008AU1	4M	IC41C16256-35K	UMC-0.21 4PDM	IBH4900P2	115x83	0.1871	5.0	0
E011AU1	4M	IC41C1664-35K	UMC-0.21 4PDM	IBF9300SC	87x63	0.1215	5.0	0

Table 3-4

[2] Bq abbreviates for becquerel, a unit to measure the radioactive strength [1 Bq= 30 alphas/min (2 pi emission rate)]; it names after the French physicist, Antoine-Henri Becquerel (1852-1908) who won the Nobel prize in Physics with Pierre and Marie Curie in 1903.

[3] Formula for geometric factor (FG):

$$FG = 1 - \cos\theta\,[1 + \frac{3}{2}\cdot\frac{L^2}{D^2}\cdot\left(\frac{\sin 2\theta}{4}\right)^2]$$

where *L, D* and θ are defined in Figure 3-11

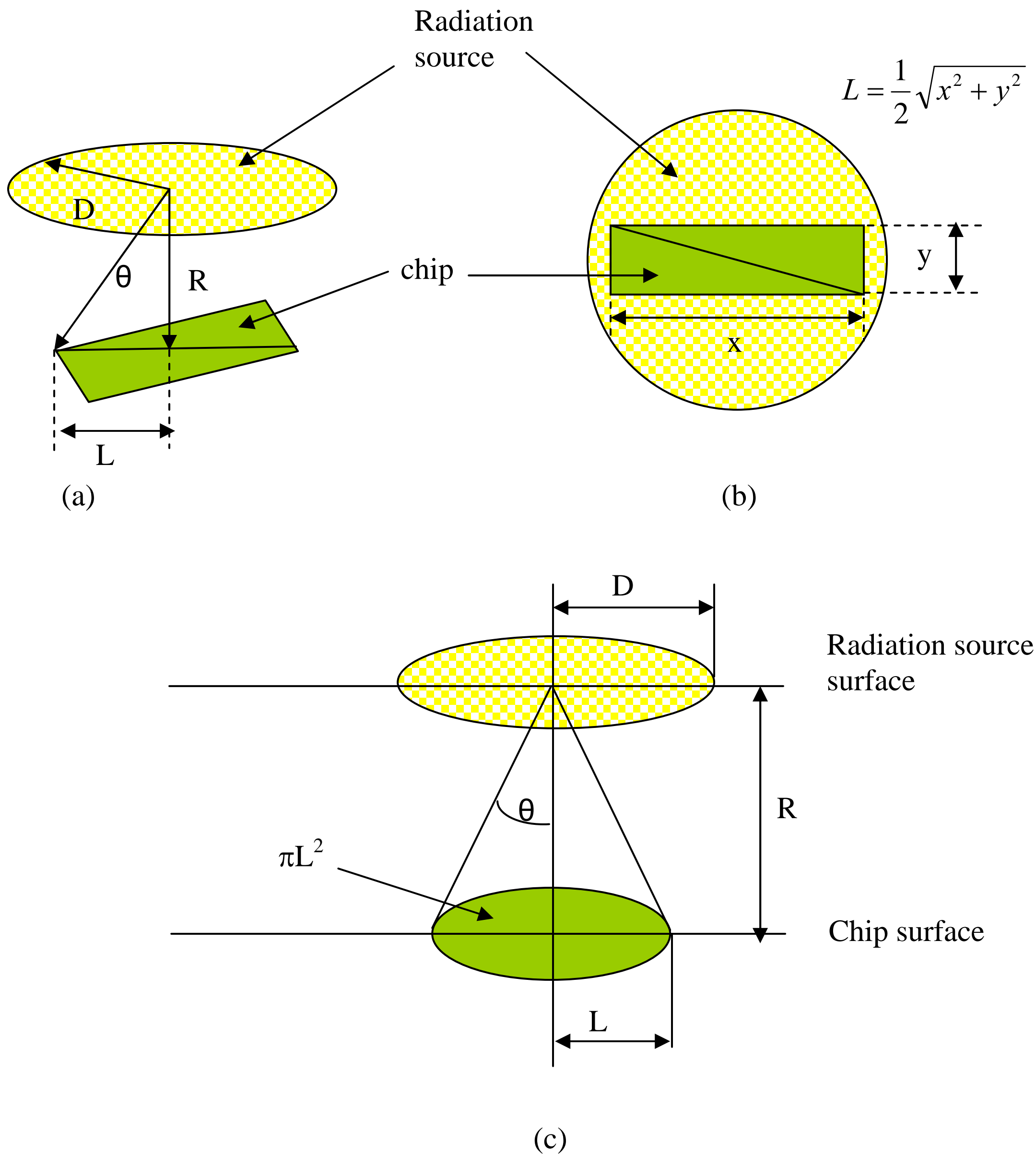


Figure 3-11 Parameters for Calculating Geometric Factor

3.2.5 Endurance Cycling and Data Retention tests
(Refer to MIL-STD-883 1033 and JEDEC 22 A117)

ISSI currently performs these two special tests on EEPROM devices for reliability evaluation.

Endurance Cycling test evaluates the quality of the tunnel oxide of EEPROM products.

Condition : Continued program-erase operation to cause charge trapping or even breakdown in the tunnel oxide

Duration : 1000K cycles at room temperature or 100K at high temperature

Failures : measure threshold shift or cell current that eventually cause failure of a

cell to retain data

Calculation : percentage of cells that cannot retain data as a function of program-erase cycling

Below show the typical endurance cycling performance of 0.35 μm EEPROM at room temperature and 125C.

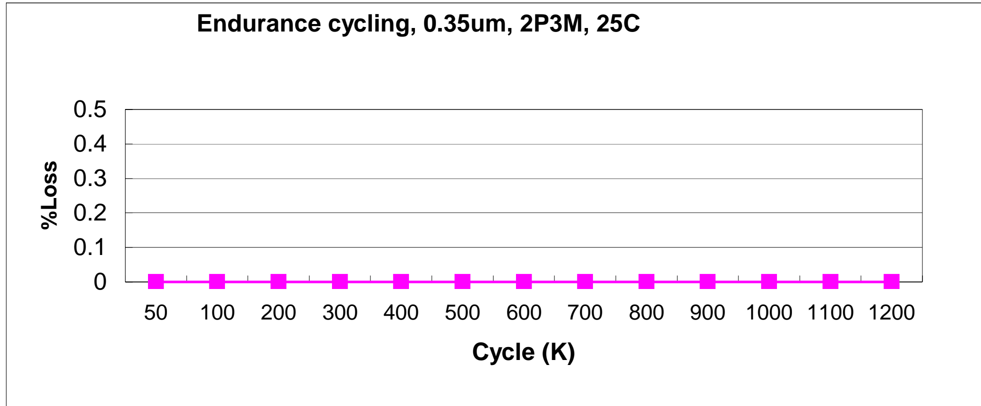


Figure 3-12 Typical Endurance Cycling performance at 25C

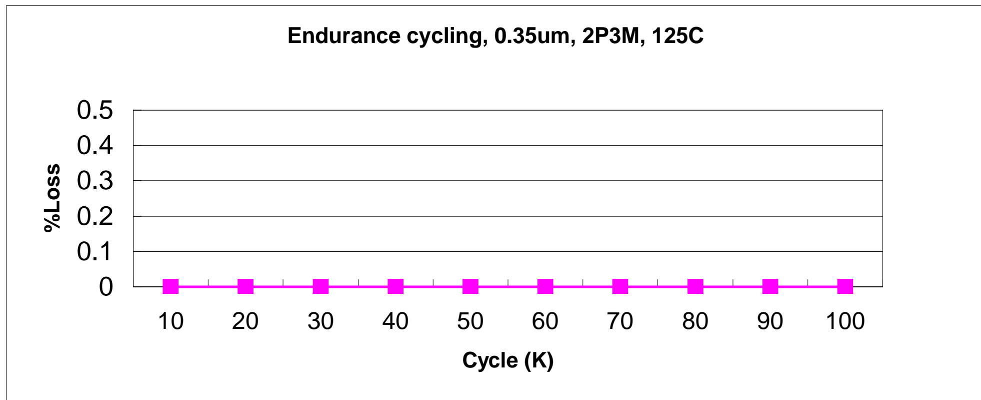


Figure 3-13 Typical Endurance Cycling performance at 125C

Data retention test measures the stability of electron in the floating gate of EEPROM products.

Condition : high temperature(typically, 150 ^{o}C) with no bias

Duration : 1000 hours

Failures : measure threshold shift or cell current that eventually cause failure of a cell to retain data

Calculation : percentage of cells that cannot retain data after baking

3.3 Package Related Test Data

(All test data are shown at the end of this chapter)

3.3.1 Pre-condition Test

Procedure:

1) baking 24 hrs at 125 ^{o}C;
2) moisture soaking at certain temperature and humidity level. For level 3: T=30 ^{o}C and RH=60%, for 192 hrs;
3) re-flowing solder IR at 240 ^{o}C/260 ^{o}C and immersing in flux for 10 seconds 3 times for regular and Pb-free packages respectively

3.3.2 Highly Accelerated Stress Test

Condition : Steady-state temperature humidity bias, voltage is normally set at 1.1× Vcc, T = 130 ^{o}C, 85% RH, 33.3 psi.
Duration: Electrical tests conducted at 100 hrs
Failure: When device fails to pass production test program
Calculation : Both temperature and humidity acceleration factors are considered for the failure rate calculation. Poisson probability distribution with confidence level = 60% is assumed.

3.3.3 Temperature Cycling Test

Condition: T = -65 ^{o}C to +150 ^{o}C temperature cycle, transition period: 5 min.
Duration: Electrical tests conducted after 250 temperature cycles.
Failure: When device fails to pass production test program
Calculation: Poisson probability distribution with confidence level = 60% is assumed.

3.3.4 Pressure Cooker Test

Condition : No bias, T=121 ^{o}C, relative humidity (RH) = 100%, pressure 15 psi.
Duration : Electrical tests conducted at 168 hrs.
Failure : When device fails to pass production test program
Calculation : Poisson probability distribution with confidence level = 60% is assumed.

3.4 Lead-free Package Roadmap

The requirements of reliability on ISSI lead-free products are similar to the test items listed in section 3.3. However some test conditions will be modified to meet customer

application conditions. Furthermore, additional items will be evaluated when appropriate, including evaluation of electrodes, evaluations regarding thermal stress and solder joint strength. The ISSI lead-free and green package roadmap is shown in Table 5-5.

3.5 Process Average Testing (PAT) , Statistical Yield Analysis (SYA) , and Junction Verification Test (JVT)

To enhance the quality control and achieve the zero defect target for automotive grade parts, we need to implement the PAT, SYA, and JVT concept in the production flow.

3.5.1 Process Average Testing (PAT)

1.) Definition:

Process Average Testing (PAT) is intended to identify Components that perform outside the normal statistical distribution.

2.) Purpose:

Every part is built with a particular design and process which, if processed correctly, will yield a certain consistent set of characteristic test results. PAT uses statistical techniques to establish the limits on these test results. These test limits are set up to remove outliers (parts whose parameters are statistically different from the typical part) and should have minimal yield impact on correctly processed parts from a well controlled process.

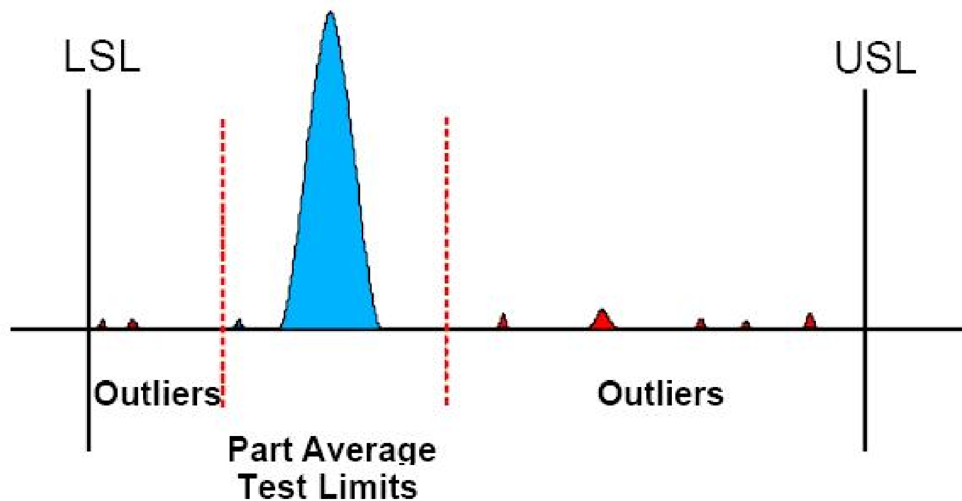


Figure 3-14 Graphical Representation of Part Average Test Limits and Outliers

History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems.

3.) Method:

a. Setting The Test Limits

$$\text{PAT Limits} = \text{Mean} \pm 6 \text{ sigma}$$

PAT test limits shall not exceed the device specification limits.

Test limits may be set in either a static or dynamic manner. New PAT limits (both static and dynamic) must be established when wafer level design changes, die shrinks or process changes have been made.

b. Static PAT limits

The static limits are established based on an available amount of test data and used without modification for some period of time.

Sample Size:

Package parts: 30 pass parts × at least 6 lots.

Wafer level: 30 pass dies from at least 5 die located × at least 6 lots.

When data from six lots is not available, data from characterization lots may be used. This data shall be updated as soon as production data is available.

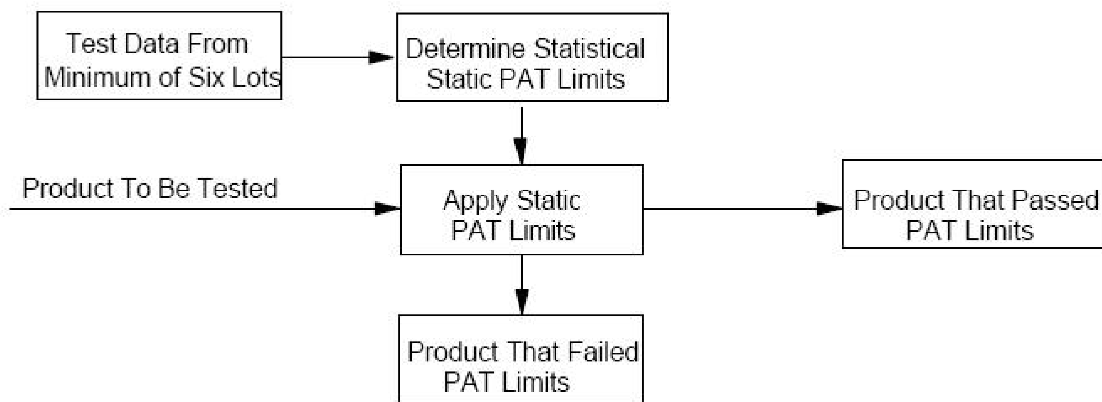


Figure 3-15 Determining Static PAT Limits

The first 6 months: PAT test limits shall be reviewed and updated as required using current data of production or the last 8 lots. Older data shall not be used.
After 6 months: The static PAT limits shall be reviewed and updated as needed on a quarterly (every 3 month) basis.

4.) Application on electrical tests

Any electrical parameter with a Cpk greater than 2.0 (CPK = 2.0 = 6σ) is considered a candidate for implementation.

PAT limits should be used for all electrical tests if possible, but shall be established for at least the important characteristics as below :

a. Junction Verification Test (JVT) - Pin Leakage Test

b. Standby power supply current (IDD or ICC)

c. IDDQ: tested with at least 70% transistor-level coverage (TLC). If the device design is not capable of being tested, then this requirement does not apply.

d.Output breakdown voltage (BVCES or BVDSS)

Output leakage (ICES or IDDS), measured at 80% of the breakdown voltage

value

Output current drive (IOUT) and output voltage levels (VOUT)

e. Additional tests:

1) Voltage Stress Test (Vs)
2) Low Level Input Current (IIL)
3) High Level Input Current (IIH)
4) Propagation Delay Or Output Response Time
5) Rise/Fall Times
6) Low Level Output Voltage (VOL)
7) High Level Output Voltage (VOH)
8) Extended Operating Tests

Extended operating tests are tests beyond the device specification requirements intended to increase the effectiveness of PAT. The following are some examples of extended operating tests: a.) voltage stress b.) low voltage operation c.) high voltage operation d.) operating frequencies above specification requirements e.) operating frequencies below specification requirements on power devices, demonstration of safe operating capability at 60% of safe operating limit, followed by leakage testing, etc.

The only restriction on these tests is that it must be demonstrated that the test does not adversely affect the reliability of the part.

3.5.2 Statistical Yield Analysis (SYA)

1.) Definition:

Statistical Yield Analysis (SYA) identifies lots of components that yield abnormal distributions, or contain abnormal failure characteristics.

2.) Purpose:

Utilizes statistical techniques to identify a wafer, wafer lot, or component assembly lot that exhibits an unusually low yield or an unusually high bin failure rate. Experience has shown that wafer and component assembly lots exhibiting these abnormal characteristics tend to have generally poor quality and can result insignificant system reliability and quality problems that impact the customer.

3.) Method:

a. 2 ways: statistical yield limits (SYL) and statistical bin limits (SBL) results. Both use test limits based on Process Average Testing (PAT) Limits.

b. Sample Size: Collect data from at least six lots and determine the mean and sigma value for the percentage of devices passing per lot and the percentage of devices failing each bin-out per lot

Early in production of a part, when data from six lots is not available, data from characterization/matrix lots may be used. This data shall be updated as soon as production data is available

c. The first 6 months: This early data shall be reviewed and updated using current

data at least every 30 days. The current data used shall include the data available since the last update or at least the last 8 lots. Older data shall not be used

After 6 months: the limits shall be updated on a quarterly (every 3months) basis

d. Setting the value for SYL and SBL

SYL_1 = Mean - 3 Sigma
SBL_1 = Mean + 3 Sigma

SYL_2 = Mean - 4 Sigma
SBL_2 = Mean + 4 Sigma

e. Disposition: Any lot that fall below SYL1 or exceed SBL1 shall be held for engineering review. In addition, lots that fall below SYL2 or exceed SBL2 may be impounded and require customer notification before release. Analysis shall be performed on failures to determine the failure mechanism causing these abnormal failure rates.

f. Records: The supplier shall maintain records on all lots that fall below SYL1 or exceed SBL1. This data shall include the root cause for the yield problem and corrective action taken to prevent reoccurrence of the problem. It should also include any special testing or screens that were performed on lot and the customer that approved the shipment of the parts in question.

4.) Customer Notification

a. Supplier shall have determined the failure mechanism and, based on his experience, determine the corrective action required to prevent a reoccurrence of the condition in future product. The supplier shall also present a plan for additional tests and screens which could provide the user with reasonable certainty that the product he receives will be at least equal to normal product.

b. The customer reserves the right to reject material that falls below SYL2 or exceeds SBL2 if the supplier data does not satisfy his concerns about the quality. The parts from the lots falling below SYL2 shall not be supplied to distributors as meeting AEC - Q100 if the supplier does not know who the customer is and customer approval can not be obtained.

3.5.3 Junction Verification Test (JVT)

1.) Definition:

Junction Verification Test (JVT) is also called “Pin leakage Test”. This test will verify that the semiconductor device pins have normal junction characteristics with respect to substrate and with respect to VDD in the case of CMOS components.

2.) Purpose:

Junction Verification Test (JVT) is used to identify IC which have wounded electrical junctions or are susceptible to EOS or a latch up condition and, perform outside the normal statistical distribution.

3.) Method:

Use the following measurement approach to establish the PAT limits for pin leakage.

a. With all pins grounded except the pin under test (PUT):

1) Force -10mA into each pin, measure the forward biased junction voltage (V F1).

2) For CMOS, also force +10mA into each pin, measure the forward biased junction voltage (VF1).

3) Test VDD (VCC) separately with respect to the substrate using -10mA, measure the forward biased junction voltage (VF2).

4) Statistically analyze this data to determine the mean for VF1 and VF2.

b. With all pins grounded except the pin under test (PUT), and using the VF1 and VF2 values determined above, measure the leakage current:

1) Apply -0.8 VF1 (80% of forward bias voltage) to each pin, measure the leakage current.

2) For CMOS, also apply +0.8 VF1 to each pin, measure the leakage currents.

3) Apply -0.8 VF2 to VDD (VCC), measure the leakage current.

4) Statistically analyze this data to determine the leakage current PAT limits.

c. After the conclusion of the final ATE test and following powering down, perform this test method to detect any possible damage that could have occurred during testing.

Chapter 4 Failure Analysis

4.1 Establishment of Failure Analysis (FA) Laboratory

4.1.1 Electrical Failure Analysis (EFA) Laboratory

Prior to 1998 -- For the purpose of engineering debug and verification of the IC's electrical characteristic in the wafer and package levels, MOSAID 3490 with probe station, HP 4145 (semiconductor parameter analyzer) and oscilloscope were acquired.

Early in 2000 -- In order to test high-speed and low power products in variable temperatures, MOSAID 4155 and thermal controller instrument were added.

4.1.2 Assembly Engineering and Chemical Laboratory

By the end of 1998 -- SAT (Scanning Acoustic Tomography), X-ray, package sawing machine, mechanical polishing machine, chemical hood, auto de-capping machine etc. were set up for the purpose of further quality improvement in packaging.

Early in 1999 -- Bonding wire defects, package delamination, die and passivation cracks, etc. could be detected by using these instruments and the information was quickly passed to the assembly house for improvement.

4.1.3 Physical Failure Analysis (PFA) Laboratory

Prior to 1999 -- PFA was performed mostly in the US based parent company, ISSI.

In 2000 -- Not only for engineering debugs but also for customer service, portable EMMI (Emission Microscope), FESEM (Field Emission Scanning Electron Microscope) equipped with EDS (Energy Dispersive Spectroscope), RIE (Reactive Ion Etching) and wire bonding system were set up sequentially to improve the PFA capability.

Early in 2001 -- ISSI FA laboratory became fully capable of performing FA works, from electrical analysis to physical failure analysis. Defects, such as gate oxide damage, via abnormality, metal damages, etc., induced during production line or field application can be detected. This FA capability helps reducing the cycle time from the product's development stage to its mature stage, improving the production yield and expediting the customer service.

4.2 Failure Analysis Function

The failure analysis function can be divided into two major categories. One is "Lab Service Items " and the other is "Internal Engineering Application". The detailed contents are listed in Figure 4-1.

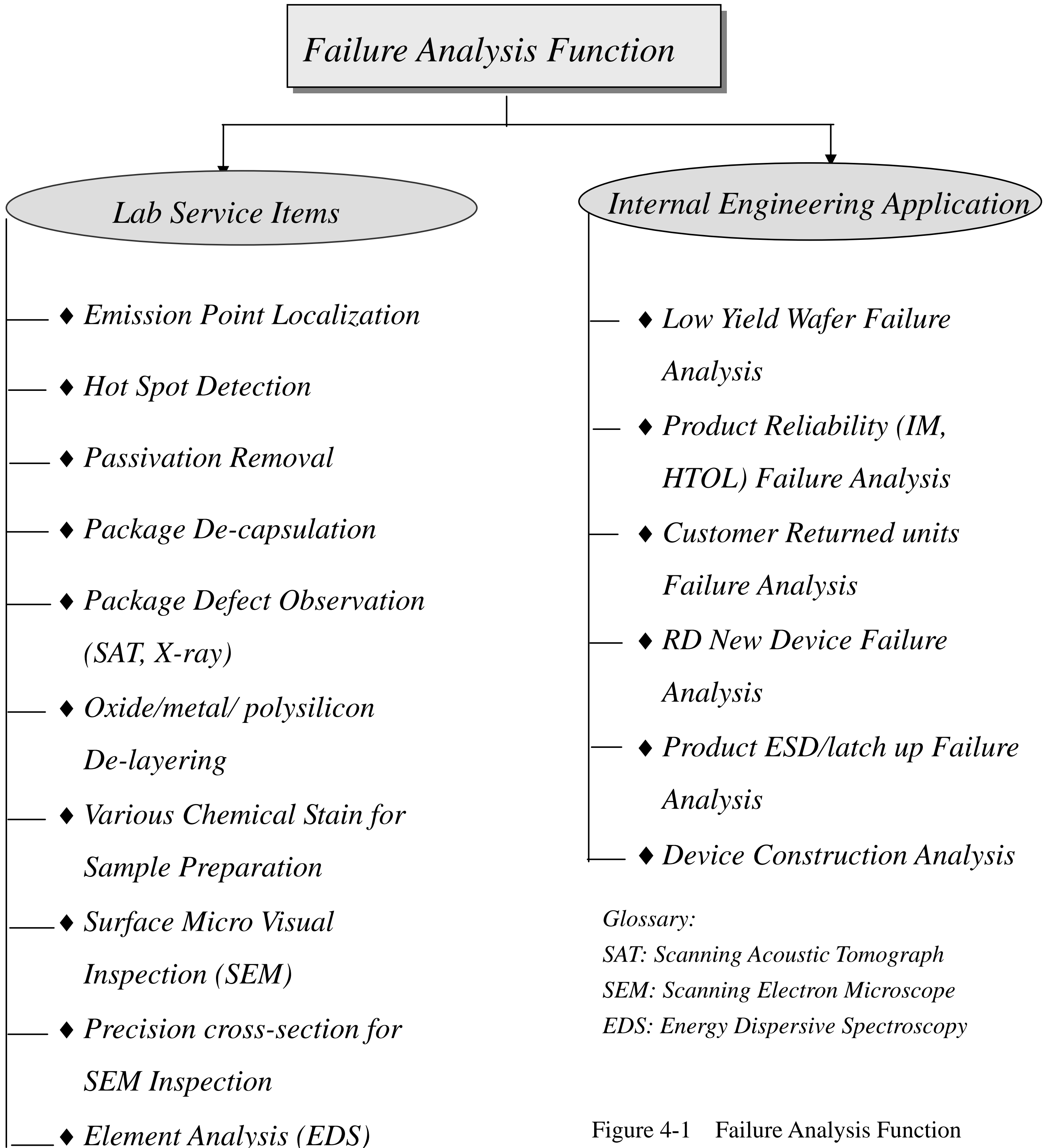
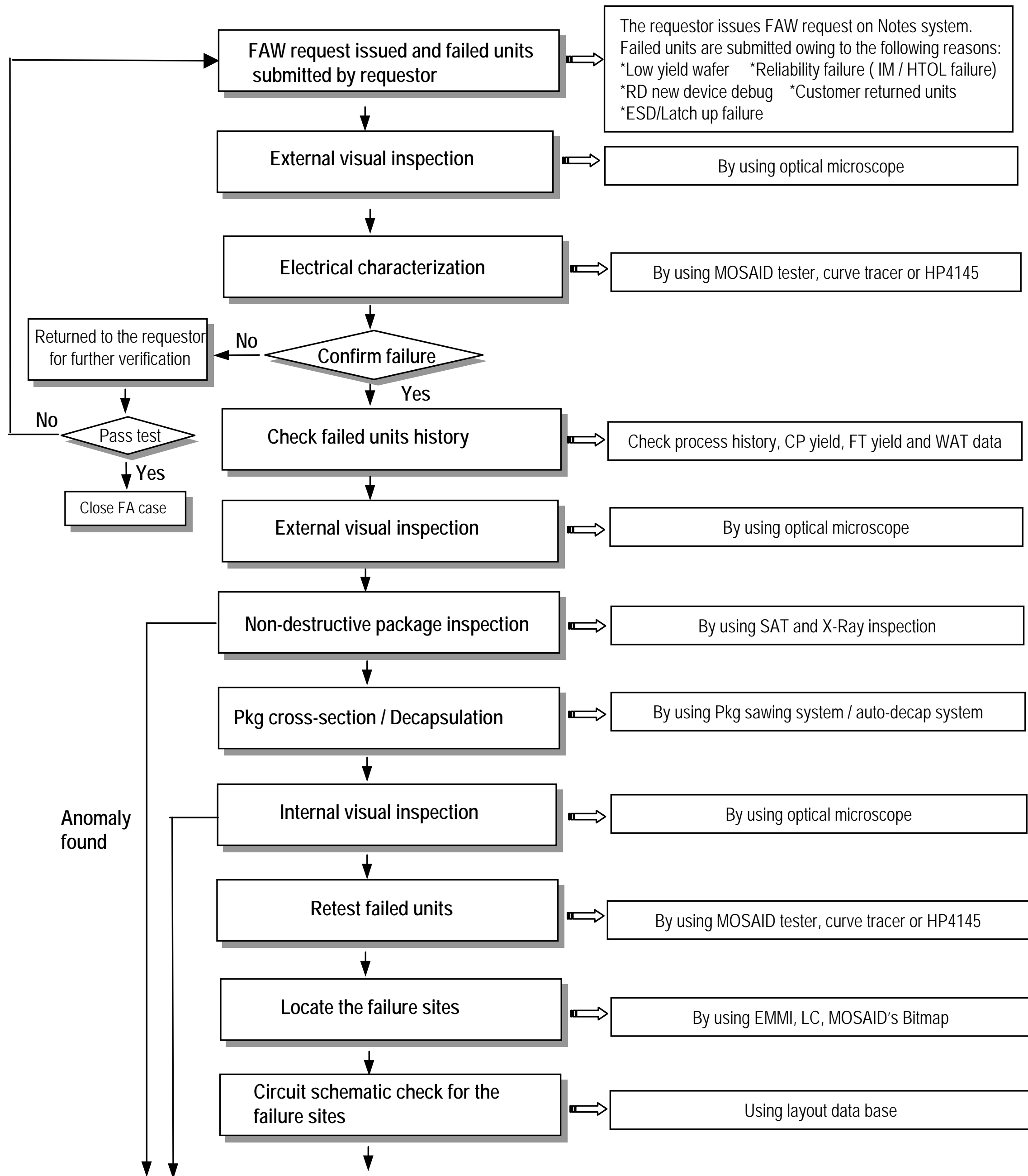


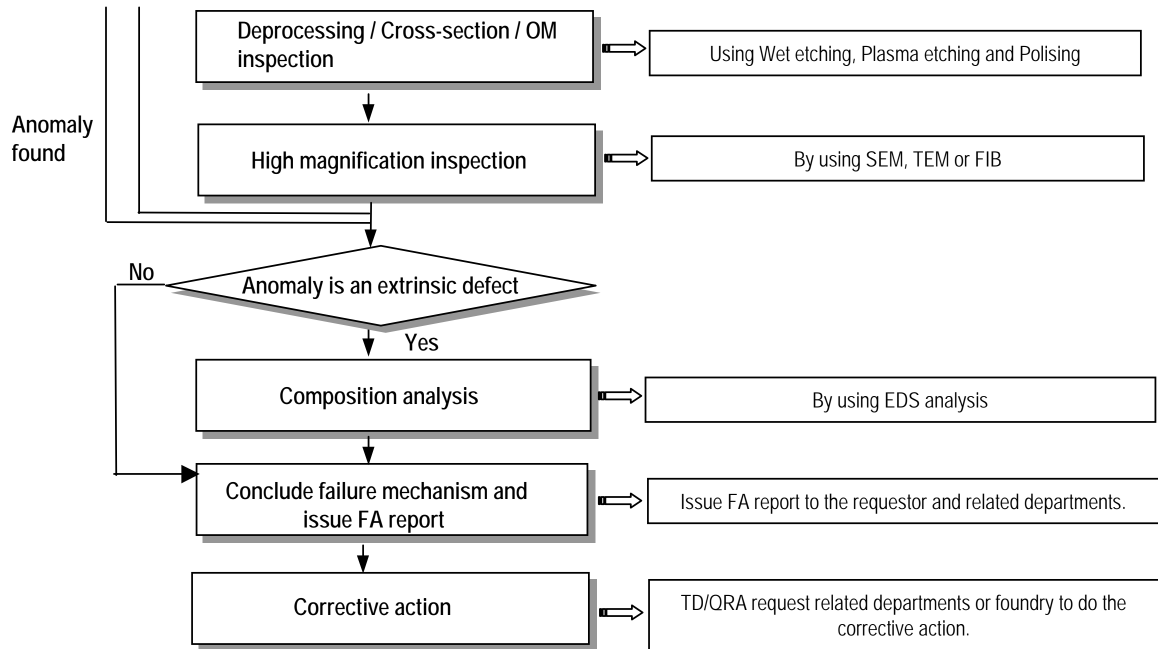
Figure 4-1 Failure Analysis Function

4.3 Failure Analysis Flow

A general failure analysis procedure is shown in Figure 4-2. The method demonstrated in the flow chart is utilized for all failure analyses.



Failure Analysis Flow



GLOSSARY:

SAT: Scanning Acoustic Tomograph
EMMI: Emission Microscopy
LC: Liquid Crystals
OM: Optical Microscopy
SEM: Scanning Electron Microscopy
TEM: Transmission Electron Microscope
FIB: Focus Ion Beam
EDS: Energy Dispersive Spectroscopy
FA: Failure Analysis

Figure 4-2 Failure Analysis Flow

4.4 Failure Analysis Instruments

As ULSI integration is becoming more complicated, analytical techniques and instruments become more advanced and dedicated in dealing with process related problems. ISSI currently has owned all necessary analytical instruments as shown in Table 4-1 in assisting the solution search for process-related problems.

Table 4-1 FA Instrument List

Category	Instrument	Principle of operation	Applications
Electrical Failure Analysis Lab	**Emission Microscope (EMMI)**	Detection of visible light, near-IR light, which are emitted at the defect sites.	Light spot localization for device leakage.
	LC detection System	Use of nematic liquid crystals for failure analysis.	Hot spot localization for device leakage.
	Engineering MOSAID 3490	Tester contains precision instrumentation combined with advanced pattern and timing facilities.	Providing functional AC and DC parametric testing capabilities.
	Engineering MOSAID 4105,4155,4205		
	Parameter analyzer (HP4145)	Applying a variable voltage or current sources to a device and acquiring the I-V curve.	Device's I-V (current-voltage) characterization.
	Semi-Auto Probe Station	Motor-driven probe station in conjunction with temperature controller for wafer.	Pad probing. Thermal stressing.
	Manual Probe Station	Probe station with anti-vibration system for wafer.	
	Pico-Probe System	Use of micro-needle for internal circuit probing of chip.	Internal circuit probing of device.
	Wire bonding System	Using depressing force and ultrasonic vibration to make the Al wire bond for the metal pad of the chip.	Wire bonding for electrical analysis of device.
	Oscilloscope		Voltage waveform measurement.
Assembly Engineering Lab	**X-ray Radiography**	Image contrast based on the attenuation of an unfocused beam from a point source.	Inspection of the wire bonding, lead frame of packages.
	Scanning Acoustic Tomographs (SAT)	Observation of the internal interface by using ultrasonic waves.	Non-destructive analysis for package's interior.

Category	Instrument	Principle of operation	Applications
Chemical Lab	**Reactive Ion Etching (RIE)**	Surface sputtering or etching of materials using accelerated ions of reactive gases.	To remove dielectric films such as Si_xN_y and Si_xO_y from devices.
	Package de-capsulator	Removal of molding compound in packages.	Decapsulation of the plastic package.
Physical Failure Analysis Lab	**Scanning Electron Microscope (SEM)**	Image from two dimensional intensity distributions of secondary electrons or back-scattering electrons from energetic e-beam.	Morphology observation. Micro structure analysis.
	Energy Dispersive Spectroscopy (EDS)	Attached to SEM equipment for detecting the radiation of characteristic X-ray.	Element detection. Composition analysis.
	Optical Microscope (OM)	Microscopy that magnifies images with a glass lens system.	For visual inspection of both wafer and package parts.
	Laser Cutting System	Using laser beam with adjustable wavelength for material removal.	Quick and easy removal of various materials on device.
	Sputtering Coater	Thin film deposition by sputtering a gold/platinum foil.	SEM specimen coating for lowering surface charge effect.
	Polisher	Grinding with diamond paper.	Specimen preparation for cross-sectional and top-view observation.
Out-sourcing Instrument	**Transmission Electron Microscope (TEM)**	Microscopy that magnifies images using diffraction of transmitted electrons.	Structure analysis. Phase identification. Defect observation. Composition analysis.
	Focus Ion Beam (FIB)	Deposition or etching of the desired patterns onto the device surface using FIB.	Device circuit repairing. Precise cross-section specimen preparation.
	Optical Beam Induced Resistance Change (OBIRCH)	Defect identification by detecting the change of resistance at defect site with scanning of a laser beam.	Localization of leakage current path Detection of vias/contacts' high resistance
	Conductive Atomic Force Microscope	Current sensing technique for electrical characterization of conductivity variations in resistive samples.	Detecting leakage or higher resistance of contact, junction etc.
	Emission Microscope with InGaAs detector	Detecting longer wavelength of near-IR light, which is emitted at the defect sites.	Light spot localization for device leakage.

Emission Microscope

Emission microscope equipped with 5 lenses (1X ~100X) and having the capability of detecting visible light and near infrared light.

Figure 4-3

Field Emission Scanning Electron Microscope

Scanning electron microscope with electron gun of cold field emission and EDX system and having the resolution of 15 Å.

Figure 4-4

Plasma Etcher (Reactive Ion Etching)

Reactive ion etching system with two separated RF generators for isotropic or an-isotropic etching of silicon dioxide, silicon nitride and other materials using fluorine based gas.

Figure 4-5

Engineering Wire-Bonding System

Engineering Al wire-bonding system with auto-height detection and auto bonding function.

Figure 4-6

Dual Wavelength Laser Cutter

Laser cutter system with laser beams at two different wavelengths and with the function of single shot and continuous shots.

Figure 4-7

Polishing System

Polishing system with the function of bi-directional (clockwise and counterclockwise) rotation.

Figure 4-8

Chapter 5.   Environmental Management

To think about and treat fairly the world we live in ...

5.1   Environmental Policy

Integrated Silicon Solution Inc. (ISSI), a technology leader, designs, develops and markets high performance semiconductors throughout the world.   ISSI acknowledges our responsibility to manage these functions in a responsible manner, endeavoring to preserve, protect and where possible enhance the environment.   To achieve these goals, we consider and control all key factors which impact the environment including the sourcing of raw material and manufacturing processes.

Our vision for the environment is C.L.E.A.N.

Continuous Improvement
    Undertake actions to prevent pollution and to maintain, review and continuously improve our environmental management system.

Legal Requirements
    Comply with all relevant environmental legislation and regulations.

Environment
    Develop, regularly review and achieve environmental objectives, targets and improvement plans.

Awareness
    Ensure all are trained and aware of the importance of their environmental responsibilities.

Naturalization
    Make the commitment to the environment a natural by-product of our processes and business activities.

All worldwide ISSI locations adhere to ISSI Environmental Policy. As prescribed by the ISO 14001:2004 Standard, ISSI Environmental Policy shall be reviewed to ensure that it :

1) Remains appropriate to the nature, scale, and environmental impacts of the organization' s activities, products, or services
2) Includes a commitment to continual improvement and prevention of pollution

3) Includes a commitment to comply with relevant environmental legislation and regulations, and with other requirements to which the organization subscribes
4) Provides the framework for setting and reviewing environmental objectives and targets
5) Is documented, implemented, maintained, and communicated to all employees
6) Is available to the public.

5.2 Environmental Management Quality Assurance

The Environment Management (EM) System defined in ISSI EM Manual is in compliance with the requirements of ISO 14001: 2004. In addition, we also rely on external subcontractors, such as wafer foundries and assembly houses. All of them are required to be ISO 14001-certified. For your reference, please see Technical Documents in the website (for member, password is needed) or contact us directly for copies of ISSI vender's ISO 14001 certificates.

5.2.1 ISO14001 Certificate

With the continuous effort in pursuing an environmentally friendly product strategy, ISSI became the first design house in Taiwan that achieved the ISO 14001:1996 standard in January 2004. The much-anticipated certificate is shown in Figure 5-1.

ISSI China followed with their certification in May of 2006. The China certificate is in Fig 5-2.

UNDERWRITERS LABORATORIES INC.

ENVIRONMENTAL MANAGEMENT SYSTEM REGISTRATION

Integrated Silicon Solution, Inc.

No. 2, Technology Rd. V
Science-Based Industrial Park
Hsin-Chu, Taiwan

Underwriters Laboratories Inc.® (UL) issues this certificate to the Firm named above, after assessing the Firm's environmental management system and finding it in compliance with

ISO 14001:2004

ENVIRONMENTAL MANAGEMENT SYSTEM

for the following scope of registration

The environmental management system of Integrated Silicon Solution, Inc. associated with the design of integrated circuit products at Hsinchu, Taiwan.

This environmental management system registration is included in UL's Directory of Registered Firms and applies to the operations of the address(es) shown above. By issuance of this certificate the firm represents that it will maintain its registration in accordance with the applicable requirements. This certificate is not transferable and remains the property of Underwriters Laboratories Inc. ®.

File Number: A12838
Volume: 1
Original Certification Date: January 16, 2004
ISO 14001: 2004 Issue Date: November 9, 2005
Revision Date: October 31, 2006
Recertification Date: January 16, 2007
Renewal Date: January 15, 2010

John H. Schmidt
Senior Vice President, Chief Development Officer

Figure 5-1 ISSI Taiwan ISO 14001: 2004 Certificate

UNDERWRITERS LABORATORIES INC.

ENVIRONMENTAL MANAGEMENT SYSTEM REGISTRATION

Integrated Silicon Solution, (Shanghai) Inc.

No.12-13, Lane 647
Songtao Rd, Zhangjiang Hi-Tech Park Pudong
New Area
Shanghai 201203

Underwriters Laboratories Inc.® (UL) issues this certificate to the Firm named above, after assessing the Firm's environmental management system and finding it in compliance with

ISO 14001:2004

ENVIRONMENTAL MANAGEMENT SYSTEM

for the following scope of registration

The environmental management system of Integrated Silicon Solution, (Shanghai) Inc. associated with the design of integrated circuits located in Shanghai, China.

This environmental management system registration is included in UL's Directory of Registered Firms and applies to the operations of the address(es) shown above. By issuance of this certificate the firm represents that it will maintain its registration in accordance with the applicable requirements. This certificate is not transferable and remains the property of Underwriters Laboratories Inc. ®.

File Number: A15376
Volume: 1
Original Certification Date: May 1, 2006
ISO 14001:2004 Issue Date: May 1, 2006
Renewal Date: April 30, 2009

John H. Schmidt
Vice President and Chief Development Officer

Figure 5-2 ISSI China ISO 14001: 2004 Certificate

5.2.2 Environmental Management Organization

ISSI Environmental Management organization is outlined as Figure 5-3.

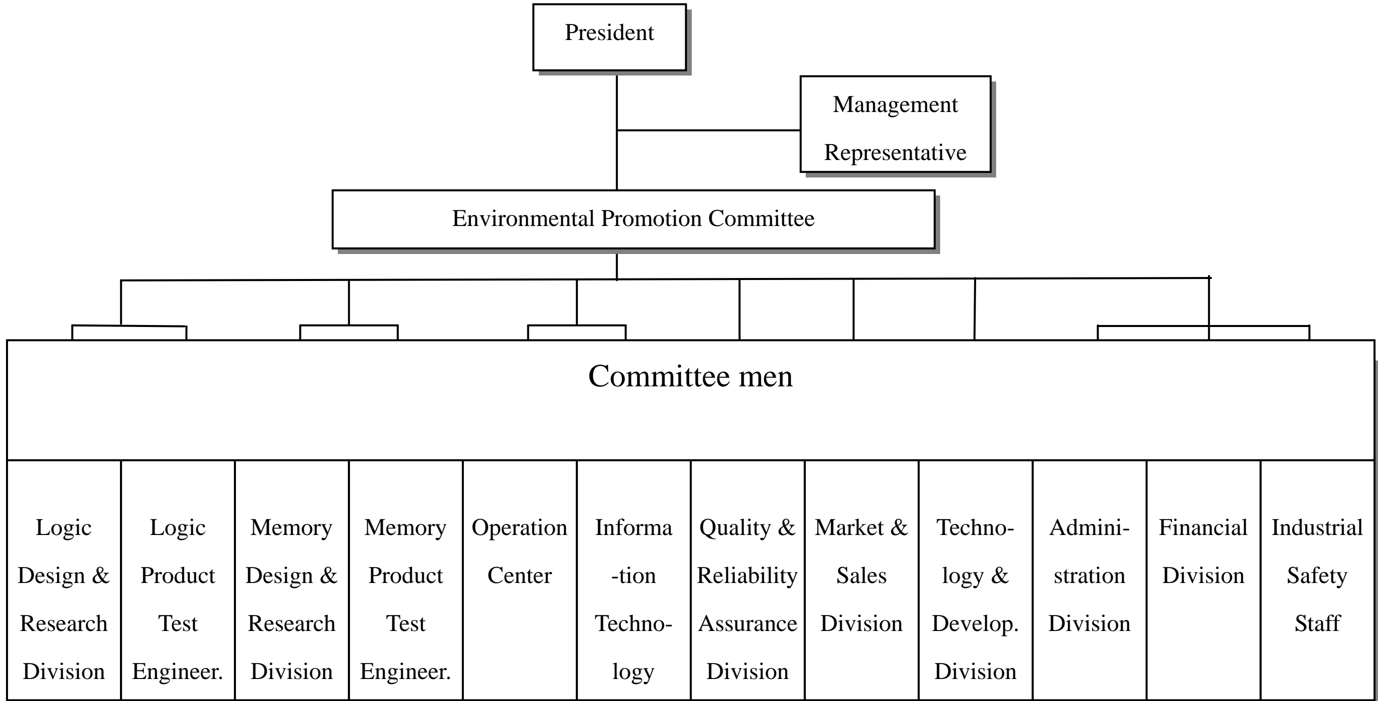


Figure 5-3. ISSI EM Organization

5.3 Environmental Substances Management

Through continuous improvement, ISSI has positioned itself to be an environmental-friendly enterprise and a green partner of all environment-concerned companies with which ISSI has a business relationship.

5.3.1 Legislation and SONY Policy

1). Europe – 1 July 2006
Total abolition of Lead, Mercury, Cadmium, Hexavalent Chromium, PFOS, PBB and PBDE has been observed since July 2006, according to the second draft of European Union order (RoHS and WEEE) for the abolishing electrical and electronic equipment.

2). Management Standards for the Restrictively Used Substances (SONY SS-00259)

No	Material/Substance Category		Threshold Level
1	Heavy Metals 重金屬	Cadmium(Cd)/Cadmium compounds	5 ppm
		Lead (Pb)/Lead compounds	100 ppm in plastics/inks
		Mercury (Hg)/Mercury compounds	Non-detected or intentionally added
		Hexavalent Chromium(Cr6+) / Hexavalent Chromium compounds	Non-detected or intentionally added
2	Chlorinated organic compounds 有機氯化合物	Polychlorinated Biphenyls (PCB)	Non-detected or intentionally added
		Polychlorinated naphthalenes (PCN; Cl > 3)	Non-detected or intentionally added
		Certain Short-Chain Chlorinated Paraffins (SCCP)	Non-detected or intentionally added
		Polychlorinated Terphenyls (PCT)	Non-detected or intentionally added
		Other Chlorinated organic compounds	Non-detected or intentionally added
3	Brominated organic compounds 有機溴化合物	Polybrominated Biphenyls (PBB)	Non-detected or intentionally added
		Polybrominated Diphenylethers (PBDE) Decabromodipbenyl ether (DecaBDE)	Non-detected or intentionally added
		Other Brominated organic compounds	Non-detected or intentionally added
4	Tributyl Tin compounds, 三丁基錫化合物 Triphenyl Tin compounds(TPT)三苯基錫化合物 Tributyl Tin Oxide (TBTO)		Non-detected or intentionally added
5	Asbestos 石棉		Non-detected or intentionally added
6	Specific aze compounds (Certain Azocourants and Azodyes) 特定偶氮化合物		Non-detected or intentionally added
7	Formaldehyde 甲		Non-detected or intentionally added
8	Polyvinyl Chloride (PVC) and PVC blends 聚氯乙烯及聚氯乙烯混合物		Non-detected or intentionally added. Tube is defined Class III as Sony spec.
9	Beryllium oxide氧化鈹 Beryllium copper? 青銅		Non-detected or intentionally added.
10	Specific phthalates (DEHP, DBP , BBP , DINP , DIDP , DNOP , DNHP) 特定鄰苯二甲酸鹽		Non-detected or intentionally added
11	Hydrofluorocarbon (HFC) , Perfluorocarbon (PFC) 氫氟碳化合物(HFC) , 全氟化碳 (PFC)		Non-detected or intentionally added
12	PFOS & PFOA 全氟辛烷硫酸 & 全氟辛酸		Non-detected or intentionally added
13	Ozone Depleting Substances (CFCs, HCFCs, HBFCs, carbon tetrachloride, etc.)		Class I: intentionally added Class II - HCFCs: 1000 ppm
14	Radioactive Substances		Non-detected or intentionally added
15	Cabolt dichloride		Non-detected or intentionally added
16	Specific benzotriazole		Non-detected or intentionally added

Table 5-1 List of “Environment-related Substances to be Controlled ”

Note: (1) Threshold level : concentration level which defines the limit (equal to or) above which the presence of a substance or material in a product or subpart must be declared based on the requirements of this specification.

(2) Intentionally Added means the deliberate use in the formulation of a product or subpart where its continued presence is desired in the final product or subpart to provide a specific characteristic, appearance, or quality. Metal plating is an example of intentional addition.

(3) Non-detected means not detected by specified inspection method/instrument.

5.3.2 Green Partner Certification

The environment-related substances shown in Table 5-1 above are controlled in the Green Partner (GP) rule. These controlled substances will be phased out gradually in ISSI depending on specific schedule in GP rule defined by customer, although the final regulation about environmental conscious substances has not been integrated in the world, like EU, Japan and US yet.

ISSI has been very proactive in the promotion of environmental-friendly products. After much effort on surveying the substance used in our packages, we have learnt the content of these substances quite well and conveyed the information to our customers. As a result, ISSI was first awarded as SONY's Green Partner in June 2003 and got renewed again in June 2005. Renewal of 2007 version is done. The current certificate is shown in Figure 5-4.

Certificate of Green Partner

SMS5567

Presented To:

USC CORPORATION

Integtrated Sillicon Solution Inc. (Taiwan)

This is to certify that you have successfully established an environmental management system that has met the requirements of the Sony Green Partner Program

Term of Validity : 2007/06/01～2009/05/31

Issued on : 2007/10/02

Approved and Issued by : Procurement Center, Sony Corporation

Toshiyuki Kikuchi

VP, Senior General Manager, Procurement Center, Sony Corporation

SONY

41684

Figure 5-4 SONY Green Partner certificate

5.3.3 Industry Definition of Lead-free & Halogen-free

1) Lead-free package :

Pb content in individual material must be less than the limited level

- IPC/JEDEC : Pb < 2000 ppm
- EU(ST/Philip/Infineon) Pb < 1000 ppm
- JEITA Pb < 1000 ppm
- **ISSI** **Pb < 1000 ppm**

2) Halogen-free package :

In addition to the requirement of Pb-free package, the Halogen-free package must reduce the content of halogen and antimony trioxide[1] to the minimum level

- Japan Electronic Insulating Material Association :
  Br, Cl, Sb < 900 ppm, respectively
- ST/Philip/Infineon Halogen (Br + Cl) < 900 ppm
  based on JPCA-ES-01-1999
- **ISSI** **Br, Cl, Sb < 900 ppm, respectively**
  Halogen (Br + Cl) < 1500 ppm

The new 'Green' definition will be followed and updated with the green standard of the environmental concerned substances changing around the world.

3) Future Material declaration requirement at an Article level for EU/REACH (Registration, Evaluation, Authorisation and Restriction of Chemicals)

The European Chemicals Agency (ECHA) has published the first candidate list of substances of very high concern (SVHC) on 28 October 2008. The list includes the original 15 substances in Table 5-2 which ECHA had proposed in the first draft. ISSI had identified all of package material is lower threshold level of the presence of SVHC from date code 0901. ISSI will pro-actively notify customer before 45 days in case of ISSI use and exceed threshold level (if >0.1 % w/w) in the future once a new candidate list of REACH which is demanded by ECHA.

REACH SVHC's (information req)	**CAS#**	**EC#**	**SVHC limit by weight of SVHC / weight of article**	**Yes or No SVHC used?**
Triethyl arsenate	15606-95-8	427-700-2	0.1%	NO
Alkanes C10-13 chloro (SCCPs)	85535-84-8	287-476-5	0.1%	NO
Hexabromocyclododecane (HBCDD)	25637-99-4	247-148-4	0.1%	NO

Lead hydrogen arsenate	7784-40-9	232-064-2	0.1%	NO
Cobalt dichloride	7646-79-9	231-589-4	0.1%	NO
Diarsenic trioxide	1327-53-3	215-481-4	0.1%	NO
Diarsenic pentaoxide	1303-28-2	215-116-9	0.1%	NO
Bis 2-ethylhexylphthalate (DEHP)	117-81-7	204-211-0	0.1%	NO
4-4'- Diaminodiphenylmethane	101-77-9	202-974-4	0.1%	NO
Benzylbutylphthalate (BBP)	85-68-7	201-622-7	0.1%	NO
Dibutylphthalate(DBP)	84-74-2	201-557-4	0.1%	NO
5-tert-butyl-2-4-6-trinitro-m-xylene	81-15-2	201-329-4	0.1%	NO
Bis(tributyltin)oxide	56-35-9	200-268-0	0.1%	NO
Sodium dichromate dihydrate	7789-12-0	234-190-3	0.1%	NO
Anthracene	120-12-7	204-371-1	0.1%	NO

Table 5-2. The 15 SVHC of the Regulation of Article 5 of (EC) No 2006/121/EC

[1] Even though antimony is not a halogen element, it is often used with halogen in the flame retardant of the molding compound. We follow ASE (Advanced Semiconductor Engineering) Group's convention to include antimony trioxide as a "halogen" element in the category of "halogen-free" package.

5.3.4 Product Composition

ISSI products are mainly dedicated to commercial and industrial markets. Few selected ones are penetrating some advanced applications. To ensure that our products can comply with the regulations of environmental protection, ISSI has established a database that contains the information of product composition by package families. This database is confirmed with related assembly houses and its information is very important because it allows us to estimate the effectiveness of re-cycle and re-use rates of products and helps us answer customer's End-Of-Life questions.

Table 5-3 below is an example sheet of material composition for thin small outline package (TSOP) family. The chemical characteristics are specified according to the components such as chip, gold wire or encapsulation. For each component, the material name, mass
percentage, element, CAS[2] number and element weight are carefully calculated. Similar sheets are available for SOP, SOJ or other package families. Please contact us if you need more information.

[2] CAS stands for Chemical Abstracts Service. It is a division of the American Chemical Society. Its registration number is widely used in MSDS (Materials Safety Data Sheet) to designate elements or compounds.

Material Composition Sheet (for IS prefix P/N) *ISSI*

Package family	Thin Small Outline Package(Type II)	54TSOP II (400mil)
Issue date	2/4/2008	
Package weight(mg)	541.200	

Composition part	Material name	Material composition(%)	Material weight (mg)	Element name	CAS No	Element composition(%)	Element weigtht(mg)	mg/kg (ppm)
Die	Silicon Chip	5.50%	29.790	Silicon	7440-21-3	99.400%	29.612	54714.73
				Aluminum	7429-90-5	0.300%	0.089	165.14
				Copper	7440-50-8	0.300%	0.089	165.14
Leadframe	A42	21.26%	115.037	Fe	7439-89-6	58.00%	66.721	123284.22
				Ni	7440-02-0	42.00%	48.316	89274.78
Die Attach Adhesive	LOC Tape	0.39%	2.136	Aromatic polyimide resin	105218-97-1	50.00%	1.068	1973.50
				polyether amideimide	Trade Secret	50.00%	1.068	1973.50
Bonding Wire	Gold Wire	0.14%	0.768	Au	7440-57-5	100.00%	0.768	1419.00
Encapsulation	Mold Compound	72.00%	389.673	Epoxy resin	Trade Secret	5.50%	21.432	39600.94
				Phenol resin	Trade Secret	4.50%	17.535	32400.77
				Carbon black	1333-86-4	0.20%	0.779	1440.03
				Silica	60676-86-0	89.80%	349.927	646575.27
Solder Plating(Pb-free)	Tin	0.70%	3.795	Sn	7440-31-5	100.00%	3.795	7013.00
Total		100.00%	541.200					

Materials Disclosure Disclaimer
Note: Even though all possible efforts have been made to provide you with the most accurate information, we can not guarantee to its completeness and accuracy due to the fact that the data has been compiled based on the ranges provided and some information that may not have been provided by the subcontractors and raw material suppliers to protect their business proprietary information. Based on the above considerations, this information is provided only as estimates of the average weight of these parts and the anticipated significant toxic metals components. These estimates do not include trace levels of dopants and metal materials contained within silicon devices in the finished products.

Table 5-3 Material Composition Sheet of 54 TSOP II

5.3.5 Lead-free Solution

5.3.5.1 Overview

Lead containing waste, disposed from PCB assembly, in landfills is eluded by acid rain, resulting in contaminated groundwater and rivers. When accumulated in the human body through drinking water or food, it will cause intellectual growth disorder in children.
The use of lead in electronic products is an important issue of global environmental protection. ISSI has received significant amount of requests regarding lead-free package demand from Japanese customers since early 2001. Consequently, ISSI has dedicated its resources to work with suppliers to provide lead-free solutions.

5.3.5.2 Background

For any alloy to be a worthwhile soldering material used in the electronic industry, it must possess certain specific qualities under the following criteria:

1) Melting Range:
   It must have a liquidus temperature that is sufficiently low so that components and boards are not damaged during soldering. In practice, this means that it must be usable at 260 degree C, which is the maximum temperature exposure limit for the majority of electronic components. Also, it must have a solidus temperature that is sufficiently high

so that during service the solder joints do not lose their mechanical strength.[3]

2) Metallurgy:

Another crucial attribute of the alloy is that it must wet the common engineering metals and metallizations (silver, copper, nickel, etc). Ideally, new alloys should also be compatible with existing fluxes, stable and non-corrosive that they can withstand the stress/strain/temperature regimes encountered in electronic applications.

3) Environment Health and Safety Issues:

The alloy and its components must be non-toxic. Similar considerations apply to the soldering fluxes and the cleaning agents.

4) Economic and Supply Issues:

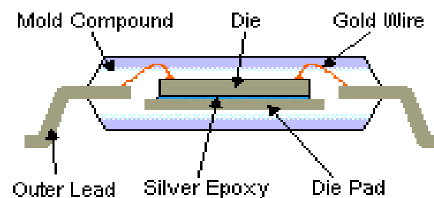
For any alloy to be considered as a potential replacement for tin-lead solder, its components must be in sufficient supply that it would not be subject to price constraints.

5.3.5.3 Lead-free Solder Solutions

There are a number of low melting point elements that can be combined to form feasible solder systems. The most practical solder systems are based on tin and bismuth or matte tin. ISSI has already provided millions of devices for both logic and memory products with lead-free external terminals. The composition and plating thickness of the lead-free solder solutions follow:

1) Outer lead:

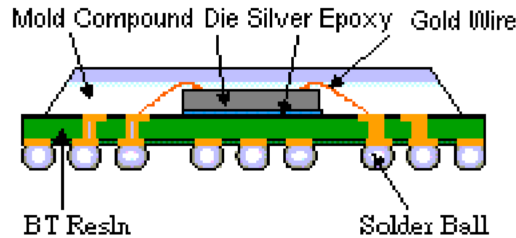
- Plating composition : Pure matte Tin (optional: 98 Sn/2 Bi plating[4] Plating thickness: 300 to 800 micro-inches(7.6 to 20.3 um). The thickness of plating of curved region of shoulder and heel region due to the plating layer is stretched and will be reduce to min 3 um after lead forming.



[3] The melting point of tin-lead eutectic at 183 provides a useful compromise between these two criteria.

[4] Sn-Bi Alloy Solders: bismuth additions to tin and other alloying agents make uniquely attractive combination for low melting point alloys which are also suitable for soldering. Bismuth also lowers the surface energy of tin and tends to improve the wetting ability of the solder. From the standpoint of wettability, Sn-Bi is superior to other solders. A drawback, however, is that it oxidizes rapidly in air. Thus stronger fluxes are required to achieve good wetting.

2) Solder ball: Composition : 96.5~95.5 Sn 3.0~4.0 Ag 0.5 Cu

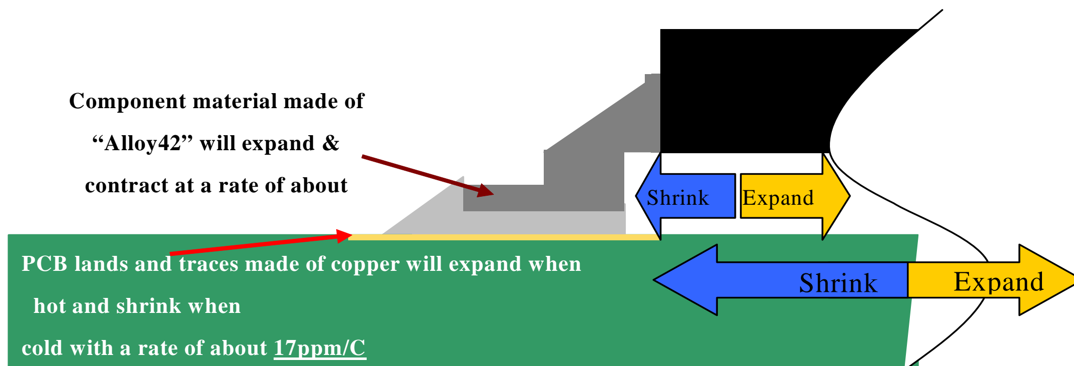


3) A copper leadframe with (NiPdAu) plating.for SDRAM (optional).

ISSI is now offering an additional option for a range of DRAMs made of a copper leadframe with Nickel-Palladium-Gold (NiPdAu) plating. The solution provides several reliability benefits, while reducing total cost of ownership.

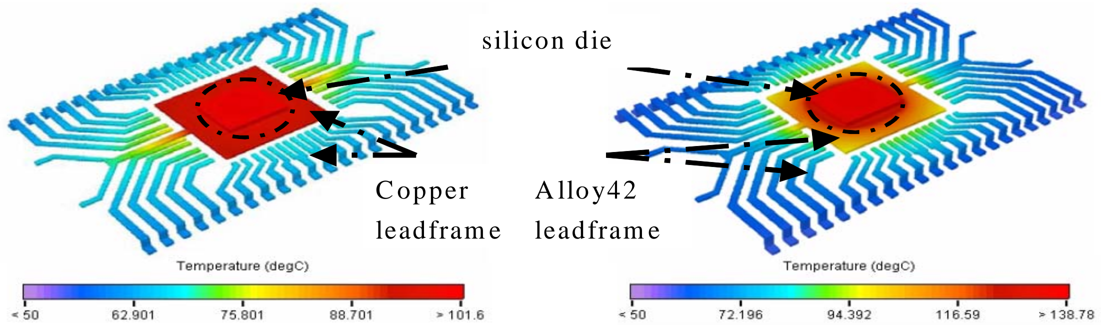
Better Joint Reliability

- The circuit boards in many applications will experience repeated temperature changes as time goes on.
- A problem can arise because every kind of material on the surface of the board has a different responsiveness to heat, often referred to as its coefficient of thermal expansion (CTE).
- Eventually, solder joints can crack from the pulling forces of expansion and contraction. When a part with a conventional Alloy42 leadframe is mounted on a copper surface, there would be approximately a 3-to-1 ratio of expansion /contraction.
- Parts made with a copper lead frame expand and contract the same amount as the copper pads, minimizing the stresses at the joints.

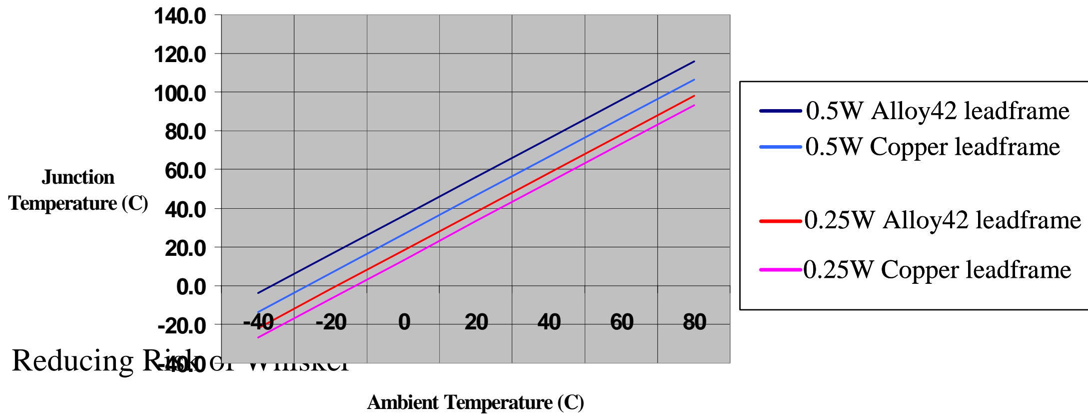


Better Thermal Dissipation

- A hypothetical analysis was made of two components that are identical, except for their leadframe materials. Both have the same power draw (1 watt), and sit in the same ambient air temperature (50°C).

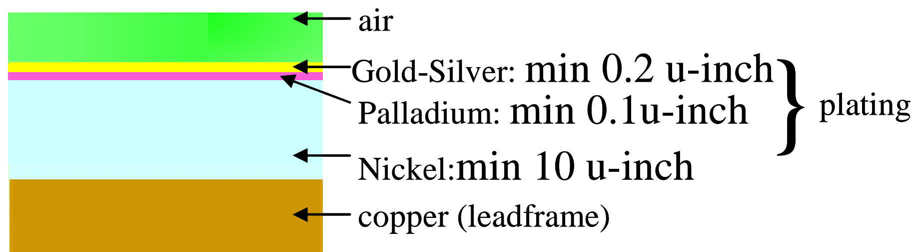


- Mostly due to the lesser thermal conductance of the Alloy42 metal, the chip on the right reaches a temperature of about 139°C, but the chip on the left sits at a relatively cooler 102°C.ith typical power use, the chip in the copper leadframe package would be about 5°C to 10°C cooler than the one in the Alloy42 package.



Reducing Risk of Whisker

iNEMI (International Electronics Manufacturing Initiative) has listed Nickel-Palladium-Gold (NiPdAu) as the most preferred plating material, due to the lack of risk of whisker formation.



(not to scale)

5.3.6 Halogen-free Solution

5.3.6.1 Overview

In epoxy molding compounds and substrates, halogens and antimony trioxide are usually

used as flame retardant to meet UL94V-0 requirement. When electronic products contain those substances are disposed and incinerated, it is possible to produce harmful dioxins.

5.3.6.2 Halogen-free Compound Status

When normal compounds are replaced with phosphorous and inorganic compounds, the moldability and reliability may be lessened. However, several industrial consortia and ISSI assemblers have evaluated halogen-free compound. Safe materials for replacement have been successfully developed with wide molding window and excellent reliability, and are commercially available now. The providers include Hitachi Chemical, Sumitomo Bakelite, ShinEtsu, etc… ISSI is currently ready to provide samples or components with halogen-free[5] compound for lead-free packages upon customer's request.

5.3.6.3 Halogen-free Substrate Status
Several industry consortia and ISSI assemblers have also evaluated halogen-free substrate. Safe materials for replacement have been successfully developed and are commercially available now. ISSI is currently ready to provide samples with halogen-free substrate for lead-free packages[6] upon customer's request.

5.3.7 Pb-free/Halogen-free Evaluation/Qualification Information

5.3.7.1 Commercial / Industrial Grade Products

The evaluation/qualification of products for general purpose is carried out in two stages. One is the standard procedure that includes preconditioning test and environmental tests. The other is the evaluation/qualification of solder plating.

1) Component or Package Level Tests
In this stage, the qualification items and procedures are similar to that of the regular packages as described in chapter 3. The details are shown in Table 5-4 and the major difference is that the IR reflow temperature of preconditioning is higher (260 °C).

Reliability Test Items	Test Method	Test Conditions	S/S	Acc No.
Preconditioning MSL 3 (Heat resistance test included)	JESD22-A113 & J-STD-020	30C / 60%RH / 192hrs + 260C IR x 3	240	0
TCT (Temp cycling)	JESD22-A104	- 65 to 150 C / 250	77	0
PCT (Autoclave or pressure cooker)	JESD22-A102	121 C / 100 %RH / 15 psi / 168 hrs	77	0
HAST	JESD22-A110	130C / 85%RH / 33.3 psi / 100 hrs	77	0

Table 5-4 Component level tests

[5] Halogen-free will cause further cost increment in comparison with lead-free. Material supply chain availability and cost concern in new material will rely on market demand in green product.

[6] The suitable halogen-free substrate for lead-free package will be available after meeting criteria specified in JEDEC level 2 or 1 with triple IR reflows @ 260 degree C.

2) Solder Plating Quality/Reliability Evaluation

The solder paste and solder plating material used in Pb-free package require higher temperature in the SMT process because these materials have higher melting point. To ensure the transition from regular package to Pb-free package will not result in detrimental failure, it is crucial to examine the mechanical properties of the solder joints, which determines the resistance to installation and handling mechanics.

Before the solder joint test, the package will go through the SMT process in which the preheating temperature is ramping up from 130 °C to 170 °C within 45 to 90 seconds. Then the package is heated to 225 °C or more within 20 to 30 seconds. The peak temperature is 230 °C or less at solder joint of terminal. The solder paste is Sn/3~4.0 Ag/0.5 Cu.

Solder joint strength tests are carried out by two items:
Item 1: lead pull strength

- all the packages will go through the pretreatment of moisture soaking at 105 °C under 100% relative humidity for 4 hours
- perform TCT test under the condition of –35 °C to 85°C with 30 minutes/cycle
- measure lead pull strength at 0, 250, 500 and 1000 cycles.

The pass criterion requires that the final lead pull strength has to exceed half of the initial values.

Item 2: cross-sectional view study

- perform SEM cross-sectional view study after 0, 250, 500 and 1000 cycles.

The pass criterion requires that the final solder joint width has to exceed half of the initial values.

5.3.7.2 Advanced Electronic Grade Products

For products used in advanced applications, we will either introduce extra test items or tighten the test conditions/criteria.

1) Component or Package Level Tests
For component level test, we add HTSL (High Temperature Storage Life) item to check the resistance of package to the prolonged high temperature storage condition.

For stricter test conditions/criteria, first of all, all the acceptance criteria allow zero failures only. In addition, final test (FT) check before and after the test is a must for all the test items involved. In some cases, FT at various temperatures are also specified such as in the PCT and HTSL tests as shown in Table 5-5.

Reliability Test Items	Reference Doc.	Test Method	Sample size/Lot	Accept Criteria	Notes
Preconditioning (Heat resistance test included)	AEC-Q100#A1	J-STD-020 & JESD22A113	231/ 3 lots	0 fails	MSL3 at least. PC performed prior to TCT, PCT and THB/HAST stresses. F/T checked before and after at room temp. Delamination from die surface is acceptable if the device can pass subsequent qualification tests.
TCT (Temperature Cycling)	AEC-Q100#A4	JESD22A104	77/ 3 lots	0 fails	checked before and after at high temp. Decap procedure on 5 units/ 1 lot after test completed, minimum wire bond pull strength (> 3 grams) on 2 corner bonds per corner and 1 mid-bond per side.
PCT (Autoclave or Pressure cooker)	AEC-Q100#A3	JESD22A102 or A118	77/ 3 lots	0 fails	121C/15psig/100 hrs. F/T checked before and after at room temp.
THB (Temp Humidity Bias or HAST)	AEC-Q100#A2	JESD22A101 or A110	77/ 3 lots	0 fails	HAST: 130C/85%RH/168 hrs with bias. F/T checked before and after at room and high temp.
HTSL (High Temp Storage Life)	AEC-Q100#A6	JESD22A103	45/ 1 lot	0 fails	Grade 2 : 125C, 1000 hrs. F/T checked before and after at room and high temp.

Table 5-5 Component level tests for advanced applications

2) Solder Plating Quality/Reliability Evaluation

Besides the aforementioned solder joint strength test, three more test items are added for advanced electronic applications. They are: the solderability and wettability test, the tin whisker check, and the electrical continuity check with Daisy Chain.

a) Solderability and wettability test

This test determines the solderability of terminals after transportation and storage. Equilibrium method will be adopted to measure the Meniscus force curve. The acceptance criterion requires the zero cross time to be less than 3 seconds.

b) Tin whisker

The extent of tin whisker growth of Pb-free package is much worse than in the regular package because the built-in stress is quite different. If this reliability issue is not well taken care of, the product might get shorted after prolonged service in the field.

The tin whisker tests will be carried out with three different approaches:

- perform TCT test under the condition of –55 °C to 85 °C with 10 minutes soak ; 3 cycles / hour for 1500 cycles .
- perform THT (High temperature humidity storage) under the condition of 30 ± 2 C° and 60 ±3% RH relative humidity for 4,000 hrs.

- perform THT (temperature humidity storage) under the condition of 55 ± 3 deg C and 85 ±3 % RH relative humidity for 4,000 hrs.

After the tests, the length of any tin whisker will be checked. The acceptance criterion is 45 µm maximum for TCT testing & 40 um for temperature humidity storage (room storage & High THT) by stereoscope at 40X or SEM at 300X above. ISSI implements annealing process to reduce tin whisker growth, For the pure matte tin of terminal is performed the heat treatment with 1hr @ 150 ℃ within 24 hrs after plating process.

c) Daisy chain
For this test, we will perform preconditioning test and TCT test for 3000 cycles. The acceptance criterion is that the electrical continuity should be guaranteed after 3000 cycles.

5.3.8 Current Status

The development work on lead-free solders has been launched by a number of organizations and institutions through either formal partnership or professional alliance in U.S., Europe and Japan. The qualified lead-free and halogen-free packages for mass production are shown in Table 5-6[7].

However, both lead-containing and lead-free packages will be provided in parallel for customers' choice.

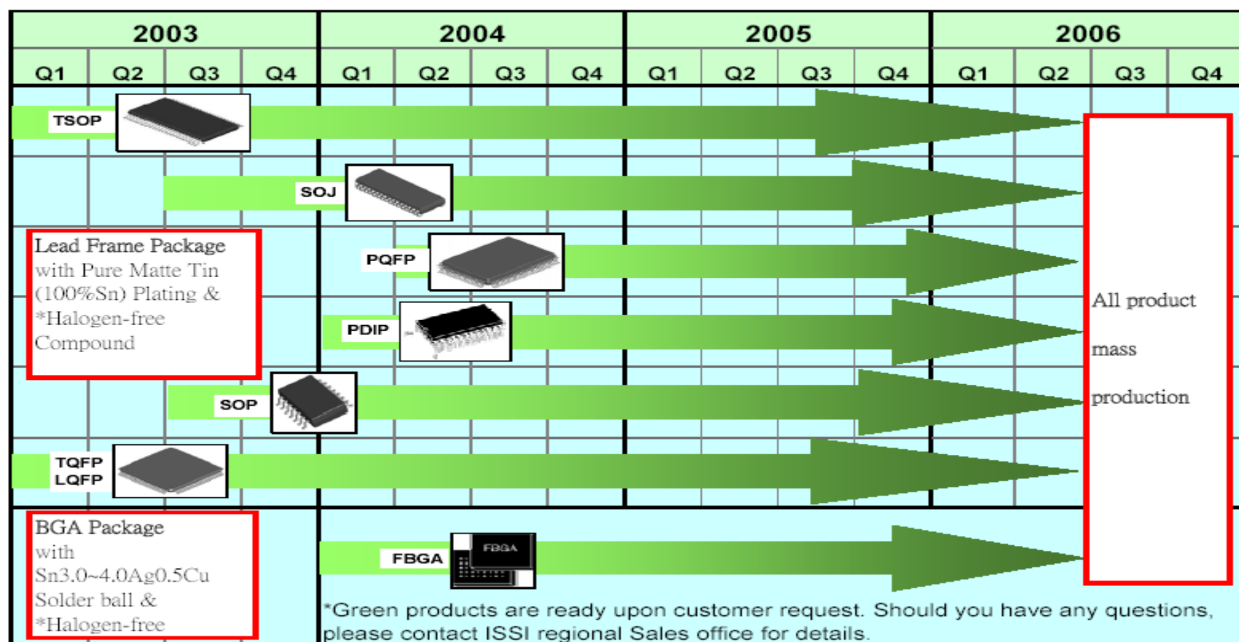


Table 5-6 Lead free and Green Package Roadmap

7 Vender may not support all the lead frames/substrates for a given package. Please contact our Assembly Engineering Group for detailed information.

5.3.9 Solder Heat Resistance for PCBA (PC Board Assembly)

Surface Mount devices (SMD) have become popular in recent years due to their advantage in high-density mounting. However, SMD package delamination often occurring between the chip/die pad and the molding compound, caused by thermal stress during mounting, has also become a problem. To assure all ISSI's products not plagued by this problem, all lead-free packages are required to meet JEDEC standard, Level 3. The recommended soldering methods and constraints are described below:

1) Reflow soldering method

Peak temperature: 260 deg C maximum, 10 seconds, soldering zone: 220 ℃ or more, 70 to 150 seconds, number of cycles: 3 cycles

2) Soldering iron method:

Temperature: 380 ℃ max., application time of soldering iron: 5 seconds maximum, number of cycles: 2 cycles

5.3.10 Lead Time from Ordering to Delivery

The maximum lead-time from ordering to delivery, for sample evaluation and mass production on unqualified lead-free and halogen-free products, is 2 and 3.5 months respectively. Should you have any comments, suggestions, or questions, please contact ISSI regional Sales office for details.

5.3.11 Discrimination Mark of Lead-free and RoHS compliance Package

1) Add an "L" or a “G” to the end of the part number. Please refer to the documents of packing and IC top mark.

2) Add lead-free discrimination stamp on dry pack, inner box and outer box (Fig. 5-5a)

3) Add RoHS label on reel, dry pack, inner box and outer box (Fig. 5-5b).

(a) (b)

Figure 5-5 Discrimination stamp & RoHS Label

5.3.12 ISSI Declaration of Compliance

Oct 31, 2008

Declaration of RoHS (including PFOS & REACH) Compliance

Dear Customer,

ISSI hereby declares that all our lead free products satisfy the following requirements/conditions:

1) Using an ''L'' or a "G" after the package type designating letter in the IS prefix or IC prefix part number for identification respectively.
2) Complying with the RoHS (EU Directive entitled "Restriction on the use of certain Hazardous Substances 2002/95/EC and 2006/122/EC") requirements and containing none of the following 7 substances: Pb, Hg, Cd, Cr(VI), PBB, PBDE and PFOS.
3) Complying with the IPC/JEDEC J-STD-020C with regard to the solder profile requirement (Max. reflow temperature 260 deg.C)
4) Complying with the 15 SVHC (substance of very high concern) of EU directive of the Regulation (EC) No 1907/2006 (REACH) as defined in table 5-2

This Declaration is made with ISSI's best commercial effort to verify the compliance, of its suppliers, with the above requirement, and is given in good faith without any responsibility or liability. The statement here above does not extend to or apply to the procedures subject to unintentional contamination, misuse, neglect, accident, improper installation or any use in violation of instructions furnished by ISSI.

This Declaration contains the entire understanding between you and ISSI with respect to this subject matter and supersedes all prior agreements, understandings and/or representations.

Please let us know if there is any further concern.

Sincerely Yours,

Shou-kong Fan
Vice President
Quality & Reliability Assurance Division