150MA DUAL CHANNEL LED DRIVER WITH FAULT DETECTION

Preliminary Information
October 2017

GENERAL DESCRIPTION

The IS32LT3126 is a dual linear programmable current regulator consisting of 2 output channels; each channel capable of 150mA. The two channels can be combined to provide a total of 300mA. It supports PWM dimming via power supply modulation (PSM). It also features ENx pins to individually enable each channel between the OFF condition and the source condition. The ENx pins also can support PWM signal to adjust the output current. An external resistors program the current level for each of the channels. The UVx pins can be utilized to set the VCC under voltage lockout of each channel to match the LED stack for high side PWM dimming operation.

The IC integrates fault protection for LED open/short, ISETx pin open/short and over temperature condition for robust operation. These failures can be reported by FAULTB pin. The FAULTB pins can all be tied together to disable the device and other IS32LT3126 devices on the same parallel circuit. In multiple LEDs per string application, the device also supports the single LED short detection by set the resister divider on the STx pins. The single LED short failure can be reported by the separated FAULTB_S pin.

The IS32LT3126 is targeted at the automotive market with end applications to include interior and exterior lighting. For 12V automotive applications the low dropout driver can support 1 to several LEDs per channel. It is offered in a small thermally enhanced eTSSOP-16 package.

FEATURES

- Dual channels: each channel can source up to 150mA and the two channels combined to source up to 300mA
- Individually programmable current via external resistor
- Individually programmable VCC under voltage lockout to match the LED stack for PSM operation
- Individual PWM dimming
- Capable of multiple IC parallel operation with fault flag linkage
- Fault protection with flag reporting:
  - Single LED short (optional to turn off all LEDs)
  - LED string open/short
  - I_{CC} set to 2mA (Max.) when fault flag is set
  - OUTx pins short to VCC/GND
  - ISETx pins open/short
  - Over temperature current rollback (no reporting)
  - Over temperature shutdown
- eTSSOP-16 packages
- Operating temperature range from -40°C ~ +125°C
- AEC-Q100 qualification in progress

APPLICATIONS

- Automotive interior/exterior lighting:
  - Turn signal light

TYPICAL APPLICATION CIRCUIT

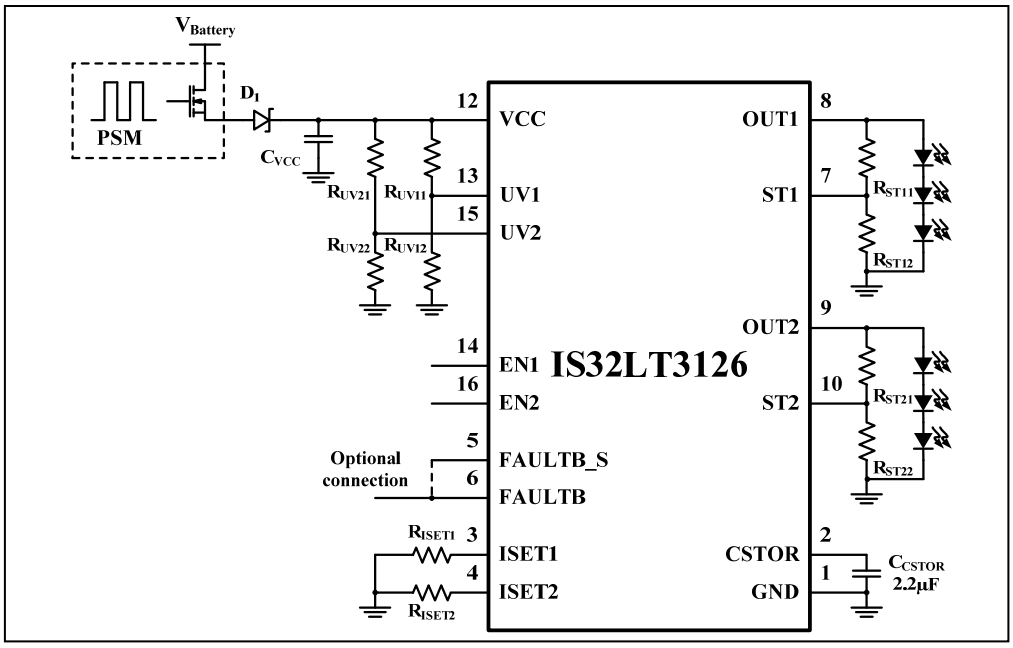


Figure 1 Typical Application Circuit

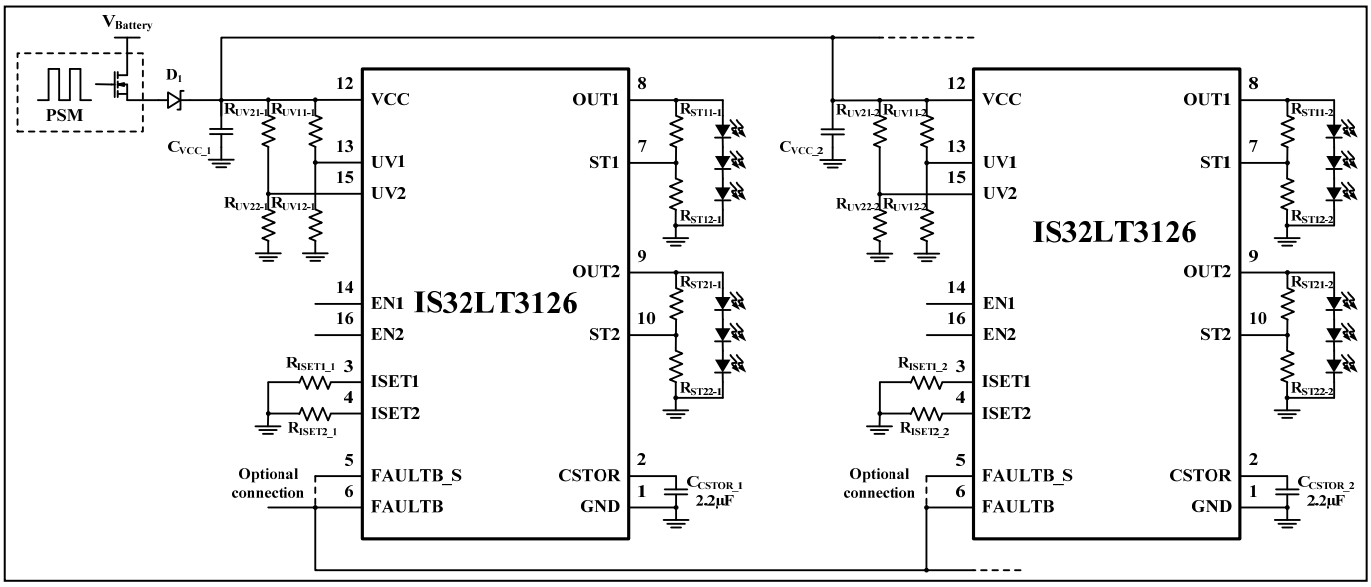
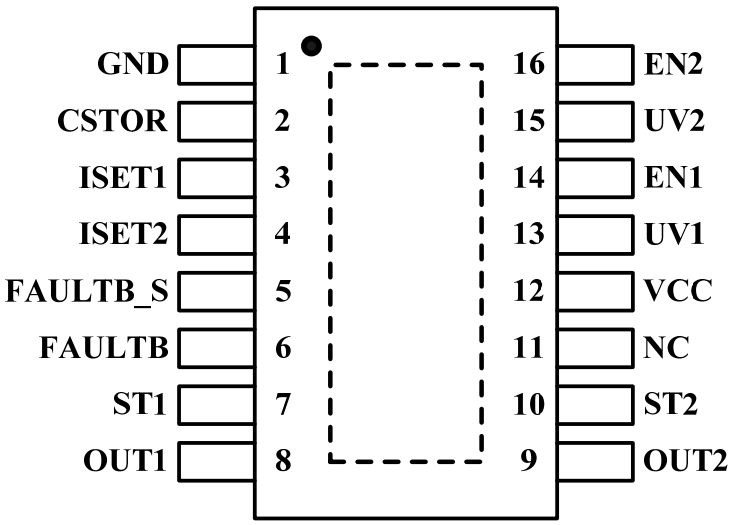


Figure 2 Typical Application Circuit (Several Devices In Parallel with FAULTB Interlinkage)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	GND	Ground.
2	CSTOR	Keep-alive capacitor to keep digital counter and fault latch alive with collapsing VCC Ground pin for the device.
3	ISET1	Output current setting for channel 1. Connect a resistor between this pin and GND to set the maximum output current.
4	ISET2	Output current setting for channel 2. Connect a resistor between this pin and GND to set the maximum output current.
5	FAULTB_S	Open drain fault reporting output with internal pull up to 5V. Indicate the fault condition of single LED short.
6	FAULTB	Open drain fault reporting output with internal pull up to 5V. Indicate the fault conditions except single LED short. This pin also is an input pin. Pull this pin low will shutdown the device.
7	ST1	LED string voltage monitor pin of OUT1 to achieve single LED short detection.
8	OUT1	Output current source channel 1.
9	OUT2	Output current source channel 2.
10	ST2	LED string voltage monitor pin of OUT2 to achieve single LED short detection.
11	NC	Not connect.
12	VCC	Power supply input pin.
13	UV1	Under voltage lockout detection pin for OUT1.
14	EN1	Enable pin of OUT1. It can be used to set OUT1 current by PWM.
15	UV2	Under voltage lockout detection pin for OUT2.
16	EN2	Enable pin of OUT2. It can be used to set OUT2 current by PWM.
	Thermal Pad	Connect to GND plane for better thermal dissipation

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY
IS32LT3126-ZLA3-TR	eTSSOP-16, Lead-free	2500/Reel
IS32LT3126-ZLA3		96/Tube

ABSOLUTE MAXIMUM RATINGS

VCC, OUT1, OUT2, EN1, EN2, UV1, UV2, ST1, ST2	-0.3V ~ +45V
ISET1, ISET2, CTSOR, FAULTB, FAULTB_S	-0.3V ~ +7.0V
Ambient operating temperature, T_A=T_J	-40°C ~ +125°C
Maximum continuous junction temperature, $T_{J(MAX)}$	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Maximum power dissipation, P_{DMAX}	2.5W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions	Value
Package Thermal Resistance (Junction to Ambient), θ_{JA}	On 4-layer PCB based on JEDEC standard	39.9°C/W
Package Thermal Resistance (Junction to Pad), θ_{JP}		2°C/W

ELECTRICAL CHARACTERISTICS

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refer to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Up Parameter						
V_{CC}	Supply voltage range		5		42	V
V_{UVLO}	VCC under voltage lockout threshold voltage	Voltage falling	4.3	4.5	4.7	V
V_{UVLO_HY}	VCC under voltage lockout voltage hysteresis			200		mV
I_{CC}	VCC supply current	V_{ENx}= High	3		5.5	mA
I_{SD}	Shutdown current in normal mode	V_{ENx}= Low, T_J= 25°C		1	2	mA
I_{SD_FLT}	Shutdown current in fault mode	V_{ENx}= High, FAULTB= Low T_J= 25°C		1	2	mA
t_{ON}	Startup turn on time	I_{OUT}= 150mA,V_{CC}= 12V V_{ENx}= High (Note 3)			40	μs
t_{SD}	The time of PWM pin keeping low to shutdown the IC			48		ms
t_P	Power cycle on (minimum)	(Note 3)		0.1		ms
Channel Parameter						
V_{ISETx}	The ISETx voltage			1		V
I_{OUT}	Output current per channel	R_{ISETx}=20kΩ, V_{HR}=1V, T_J=25°C	94	100	106	mA
		R_{ISETx}=20kΩ, V_{HR}=1V T_J = -40°C ~ +125°C	90	100	110	
V_{DO}	Minimum dropout voltage	V_{CC} – V_{OUT}, I_{OUT}= -150mA			1000	mV
		V_{CC} – V_{OUT}, I_{OUT}= -100mA			700	

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refer to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OUT_R}	Output current per channel range	R_{ISETx}= 80kΩ, I_{OUT}=-25mA R_{ISETx}= 13.33kΩ, I_{OUT}=-150mA	25		150	mA
I_{OUT_L}	Output limit current	R_{ISETx}=5kΩ	170	230	290	mA
ΔI_{OUT}	Current matching	R_{ISETx}=20kΩ, T_J=25°C	-4		4	%
t_{SL}	Current slew time	Enable by ENx pin, c urrent rise/fall between 0%~100%		4		μs
I_{LEAK}	Leakage current per channel	V_{ENx}=Low, V_{OUT}=0V, V_{CC}=42V			1	μA
Fault Protect Parameter						
t_{FD}	Fault deglitch time	*Fault must be present at least this long to trigger the fault detect		25		μs
V_{FAULTB}	FAULTB pin voltage	Sink current=20mA			0.4	V
R_{FAULTB}	FAULTB pin internal pull up			210	300	KΩ
V_{FAULTB_IH}	FAULTB pin input high enable threshold				2	V
V_{FAULTB_IL}	FAULTB pin input low disable threshold		0.8			V
V_{FAULTB_S}	FAULTB_S pin voltage	Sink current=20mA			0.4	V
V_{SCD}	OUTx pin short to GND threshold	Measured at OUTx	1.0	1.2	1.5	V
V_{SCD_HY}	OUTx pin short to GND hysteresis	Measured at OUTx		300		mV
V_{OCD}	OUTx pin open threshold	Measured at (V_{CC}-V_{OUTx})	150	225	300	mV
V_{OCD_HY}	OUTx pin open hysteresis	Measured at (V_{CC}-V_{OUTx})		100		mV
I_{CSTOR}	CSTOR pin leakage current	V_{CSTOR}=5.5V		1	10	μA
T_{RO}	Thermal rollback threshold	(Note 2)		145		°C
T_{SD}	Thermal shutdown threshold	(Note 3)		165		°C
T_{HY}	Over-temperature hysteresis	(Note 3)		25		°C
Logic Input						
V_{EN}	ENx input voltage threshold	Voltage rising	1.18	1.23	1.28	V
V_{ENHY}	ENx input hysteresis	(Note 3)		40		mV
f_{PWM}	PWM frequency to ENx	(Note 3)			1	kHz
V_{UV}	UVx input voltage threshold	Voltage rising	1.18	1.23	1.28	V
V_{UVHY}	UVx input hysteresis			40		mV
V_{ST}	STx input voltage threshold	Voltage rising	1.12	1.16	1.20	V
V_{STHY}	STx Input hysteresis			40		mV
R_{STPL}	STx pull up resister	V_{ST}=1V		500		KΩ

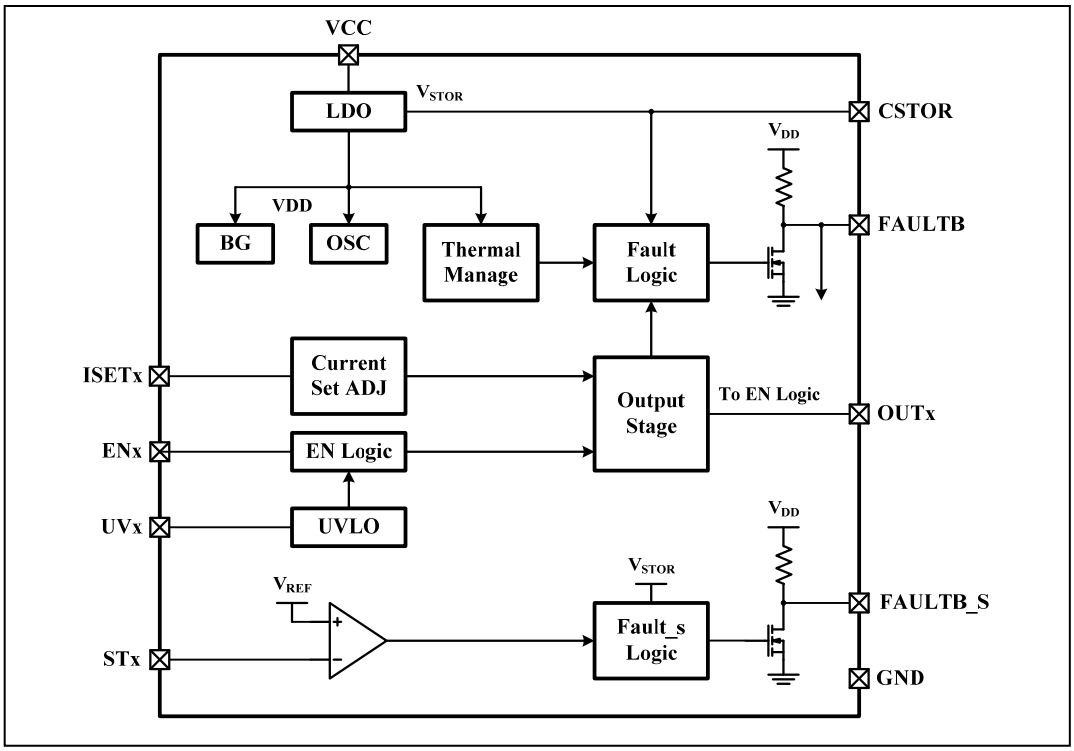
Note 1: Output current accuracy is computed as 100×[1 - 2×I_{OUTx}/(I_{OUT1}+I_{OUT2})]. Output current channel to channel match is computed as 100 × [Max (|I_{OUTx}– $I_{OUT(AV)}$|) / $I_{OUT(AV)}$], where $I_{OUT(AV)}$ is the average current of all active outputs.

Note 2: Output current accuracy is not intended to be guaranteed at output voltages less than 1.8V.

Note 3: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS (TBD)

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3126 is a 2-channel linear current driver optimized to drive an automotive interior and exterior lighting which is dimming via Power Supply Modulation (PSM).

The dual linear programmable current regulator consists of 2 output channels; each channel capable of 150mA. The output is set by a single reference resistor (R_{ISET}) for both channels. Current is matched in each string eliminating the need for ballast resistors.

OUTPUT CURRENT SETTING

A single programming resistor (R_{ISET}) controls the maximum output current for each channel. The programming resistor may be computed using the following equation (1):

$$R_{ISET} = \frac{2000}{I_{SET}} \qquad (1)$$

(13.33kΩ≤R_{ISET}≤80kΩ)

The device is protected from an output overcurrent condition caused by a too low value R_{ISET}, by internally limiting the maximum current to I_{OUT_L}.

In case of one channel is unused, the OUT pin should be tied to VCC pin to prevent unwanted fault reporting.

POWER SUPPLY MODULATION DIMMING

The IS32LT3126 can operate with Power Supply Modulation (PSM) where the device's power supply is pulse width modulated to achieve LED dimming. The IS32LT3126 stability is not affected by operation with PSM. To get better dimming linearity, the PSM frequency can be in the range of 100Hz to 300Hz, (200Hz Typ.) and input capacitor, C_{VCC}, should be low value to ensure rapid discharge as PSM low period. Recommend to use 0.1μF for it.

CSTOR OPERATION

To keep the IC operating normally during condition of PSM when V_{CC} goes to zero, CSTOR capacitor provides the keep-alive current needed to power the digital counter and the fault flag circuits. A capacitor 2.2μF is recommended.

ENx PINS OPERATION

The ENx voltage is higher than V_{EN} to enable the IC and drop V_{ENHY} to disable IC. The ENx pins of the IS32LT3126 can accept a PWM signal to implement LED dimming. LED current may be computed using the following Equation (2).

$$I_{LED} = I_{MAX} \times D_{PWM} \qquad (2)$$

I_{MAX} is computed using Equation (1). To guarantee a reasonably good dimming effect, recommend PWM frequency in the range of 100Hz ~ 1kHz. Driving the ENx pins with a PWM signal can effectively adjust the LED intensity. The PWM signal voltage levels must meet the ENx pins input voltage levels, V_{EN}. Tie them to VCC pin via a resister when ENx pins are unused. Please do not leave it floating.

UVx PINS OPERATION

The IC has an internal VCC UVLO set at V_{UVLO}. However, it may be desirable to externally set an UVLO to track the number of LED's used in the string. For PSM dimming application, the higher UVLO will track the PSM off time to a pre-determined VCC level. In addition, it is necessary to prevent false LED open detection due to the LED string loses its headroom, such as VCC rises up from zero during power up or PSM dimming. The UVx pin can be used to set a VCC under voltage lockout threshold via a resistor divider for each channel.

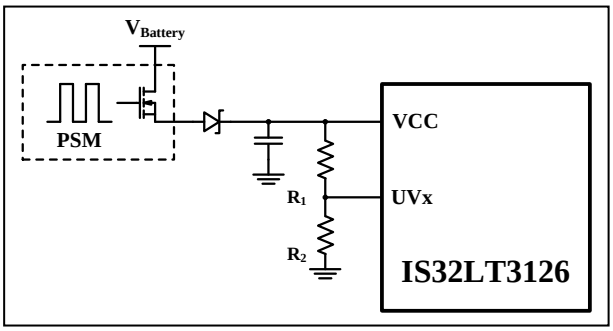


Figure 3 UVx Pins Operation

This external UVLO threshold voltage can be computed using the following equation (3):

$$V_{CC\_UVLO} = V_{UV} \times \frac{R_1 + R_2}{R_2} \qquad (3)$$

If the external UVLO is unused, UVx pins should be tied to VCC pin via a resister. Please do not leave it floating.

To prevent false open detection, the external UVLO threshold voltage should be set at:

$$V_{CC\_UVLO} > V_{LED\_MAX} + V_{OCD} \qquad (4)$$

Where V_{LED_MAX} is the maximum LED string forward voltage on the output channels.

STx PINS OPERATION

IS32LT3126 device features one LED shorted detection by set the resister divider on the STx pins. In the case of any single LED shorted results in that the STx pins voltage drops below the threshold voltage V_{ST} and remains for t_{FD}, the FAULTB_S pin pulls low to report the failure to host and all channels continue sourcing current. If FAULTB_S pin is tied to FAULTB pin, the FAULTB_S pin pulls down the FAULTB pin together that turns off the no fault condition channel but keep 4mA sourcing on fault channel for recovery

detection. In multiple LEDs per string application, set the detection threshold voltage V_{DT} into below voltage range:

$$(N-1)\times V_{F\_max} < V_{DT} < N\times V_{F\_min} \qquad (5)$$

Where, N is the LED amount in the string. V_{F_max} and V_{F_min} are the maximum and minimum forward voltage of single LED.

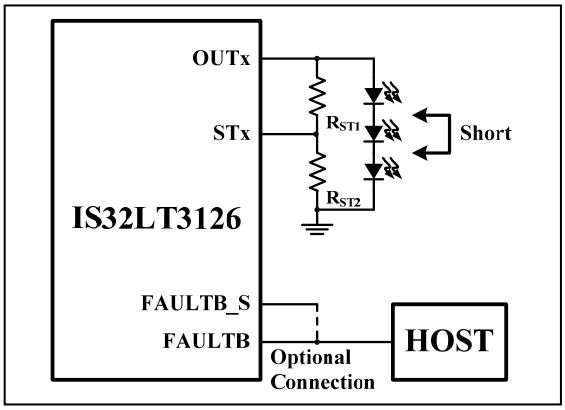


Figure 4 STx Pins Operation

The detection threshold voltage V_{DT} is calculated by the following equation:

$$V_{DT} = V_{ST} \times \frac{R_{ST1} + R_{ST2}}{R_{ST2}} \qquad (6)$$

If one LED shorted detection is unused, the STx pins should be directly tied to according OUTx pins.

OUTPUT STATE DETECTION AND FAULT DIAGNOSTIC

IS32LT3126 offers a fault diagnostic function. Output shorted to GND/VCC, open load or ISET pin short/open will trigger this function.

An output shorted to GND or VCC fault is detected if the OUTx pin voltage drops below the short detect voltage threshold V_{SCD} or VCC to OUTx drop voltage is lower than V_{OCD} and remains below the threshold for t_{FD}. Then the fault channel will change to source a 4mA current for recovery detection and the another channel will turn off. The FAULTB pin will pull low to indicate the fault condition. This state will recovery after short condition is removed.

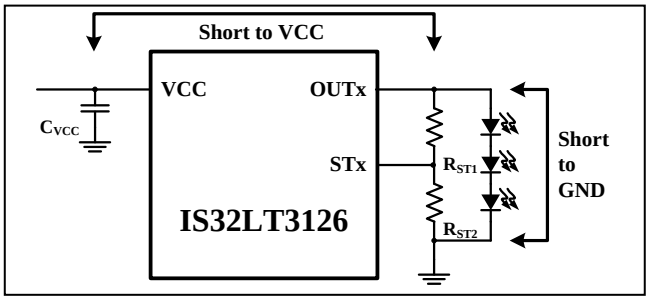


Figure 5 OUTx Pins Shorted Operation

In the event of any channel is open load and OUTx pin voltage will go up close to V_{CC}. If VCC to OUTx drop voltage remains below the threshold V_{OCD} for t_{FD}, the fault channel will change to source a 4mA current for recovery detection and the another channel will turn off. The FAULTB pin will pull low to indicate the fault condition. The state will recovery after the open condition is removed.

If the ISETx pin is either shorted or open, the FAULTB pin will pull low to assert the fault and the both channels will turn off. The difference is that ISET pin open fault will retry after R_{ISET} restored, while the ISET short fault will recovery after short condition is removed.

FAULTB PARALLEL INTERCONNECTION

For LED lighting systems which require the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection with multiple IS32LT3126 devices as shown in Figures 2. A detected fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn off them. This satisfies the “One-Fail-All-Fail” operating requirement. The IS32LT3126 will release the FAULTB bus when external circuitry pulls the FAULTB pin high, but the individual device (the chip which fault active) couldn’t release.

THERMAL ROLLBACK OF OUTPUT CURRENT

To protect the IC from damage due to high power dissipation, the temperature of the die is monitored. When the temperature of the die is below the thermal rollback start threshold of 145°C (Typ.), the output current maximum is the value set by the selection of R_{ISET}. When the die temperature is between the thermal rollback start threshold 145°C (Typ.) and the over temperature shutdown threshold 165°C (Typ.), the output current decreases linearly from the maximum value. During the rollback, the FAULTB pin will not assert this fault.

The rollback slope is related to ISET value. When I_{SET}=25mA, the rollback slope is about 3.1%/°C. When I_{SET}=150mA, the rollback slope is about 2.3%/°C.

THERMAL SHUTDOWN

In the event that the die temperature exceeds 165°C, the device will goes into shutdown mode. Both channels (OUTx) will turn off. The FAULTB pin will pull low and latch low to indicate the fault. At this point, the IC begins to cool off. Any attempt to enable one or both of the channels back to the source condition before the IC cooled to T_J<140°C will be blocked and the IC will not be allowed to restart. This state will not resume until junction temperature is below 140°C.

Table 1 Fault Table

Fault Type	Fault Condition	Fault channel	Another channel	FAULTB	FAULTB_S	Recovery
ISETx open	ISETx pin current close to zero	Off	Off	Low	High	ISETx pin current goes back high
ISETx short	ISETx pin voltage close to zero	Off	Off	Low	High	ISETx pin voltage goes back high
LED string open (OUTx shorted to VCC)	$(V_{CC}-V_{OUTx})<V_{OCD}$	4mA for recovery detection	Off	Low	High	$(V_{CC}-V_{OUTx})>(V_{OCD}+V_{OCD\_HY})$
LED string shorted (OUTx shorted to GND)	$V_{OUTx}<V_{SCD}$	4mA for recovery detection	Off	Low	High	$V_{OUTx}>(V_{SCD}+V_{SCD\_HY})$
One LED shorted	STx pin voltage drops below V_{ST}	Keep normal sourcing		High	Low	STx pin voltage rises above V_{ST}
	FAULTB_S tied to FAULTB and STx pin voltage drops below V_{ST}	4mA for recovery detection	Off	Pulled low by FAULTB_S	Low	STx pin voltage rises above V_{ST}
Thermal rollback	$T_J>T_{RO}$	Output current linearly decreases following T_J		High	High	$T_J<T_{RO}$
Thermal shutdown	$T_J>T_{SD}$	Off		Low	High	$T_J<(T_{SD}-T_{HY})$

THERMAL CONSIDERATIONS

The package thermal resistance, $R_{\theta JA}$, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The $R_{\theta JA}$ is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, $R_{\theta JA}$, as in Equation (7) and (8):

$$P_D = V_{CC} \times I_{CC} + \sum_{x=1}^{2}(V_{CC} - V_{OUTx}) \times I_{OUTx} \quad (7)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times R_{\theta JA} \quad (8)$$

Where V_{CC} is the supply voltage, V_{OUTx} is the OUTx voltage and T_A is the ambient temperature.
When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (9):

$$P_{D(MAX)} = \frac{125°C - 25°C}{R_{\theta JA}} \quad (9)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{39.9°C/W} = 2.5W$$

Figure 6, show the power derating of the IS32LT3126 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.
The thermal resistance is achieved by mounting the IS32LT3126 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3126. Multiple thermal vias, as shown in Figure 7, help to conduct the heat from the exposed pad of the IS32LT3126 to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink.

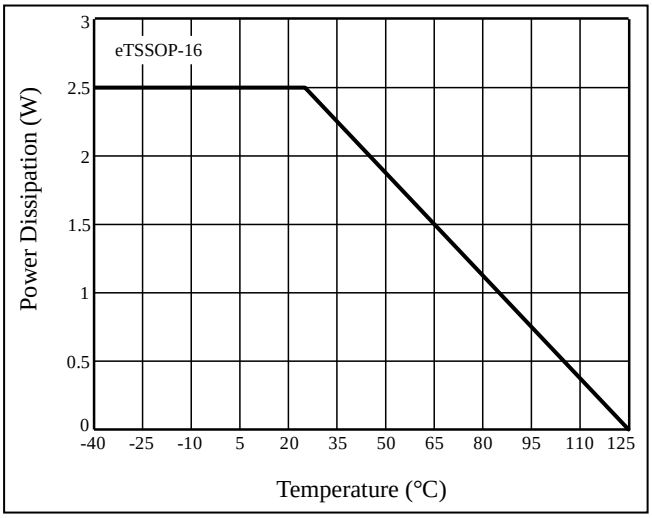


Figure 6 Dissipation Curve

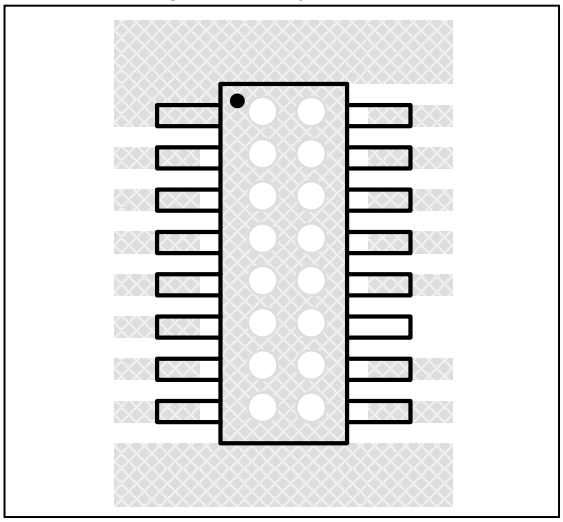


Figure 7 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

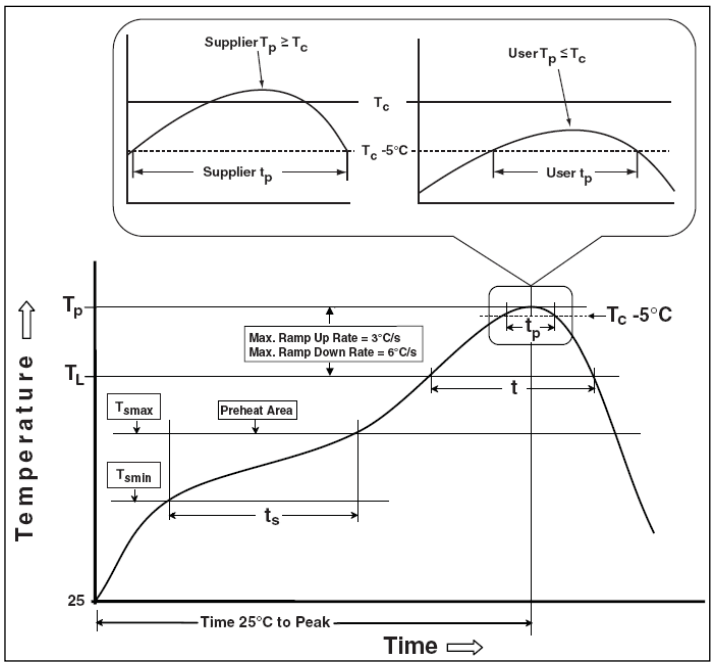
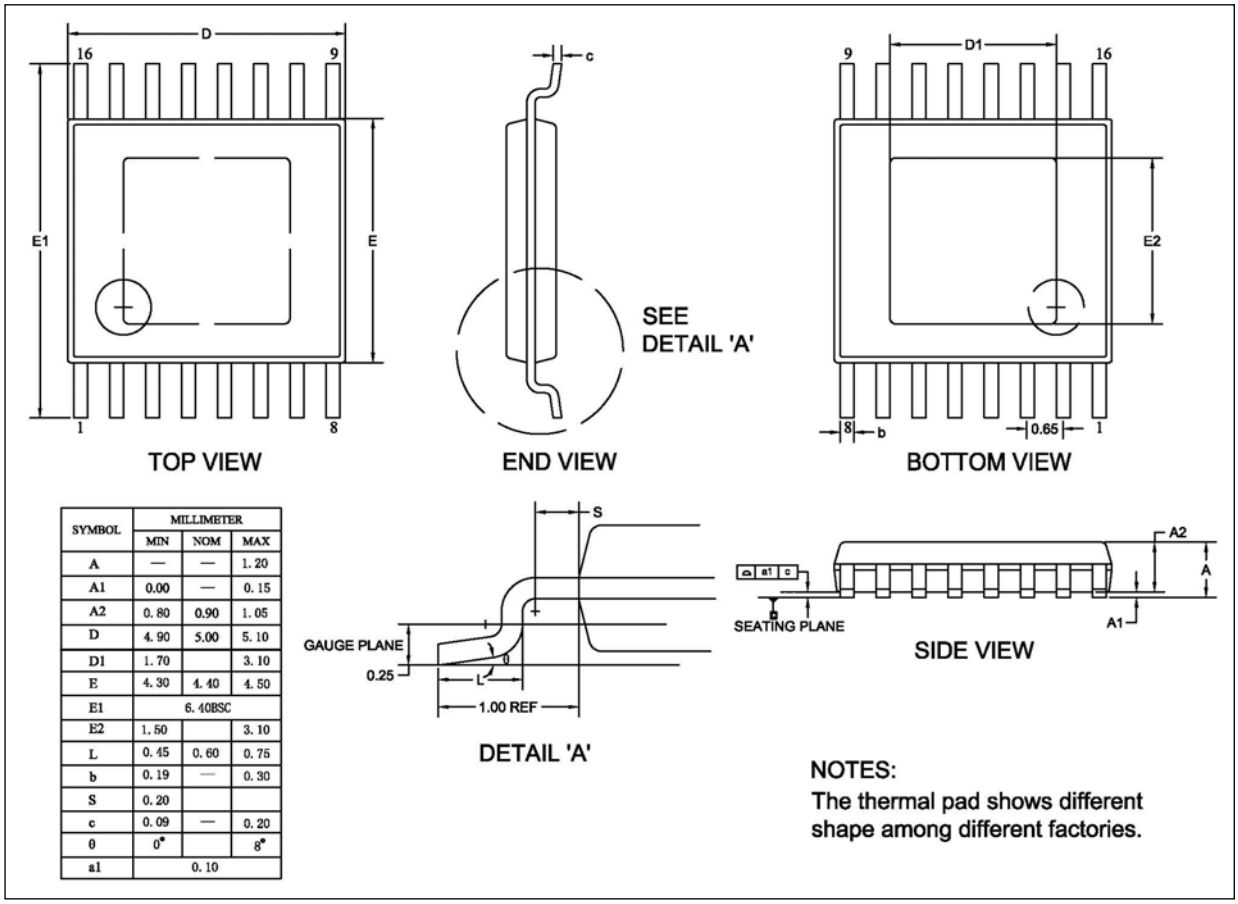


Figure 13 Classification Profile

PACKAGE INFORMATION

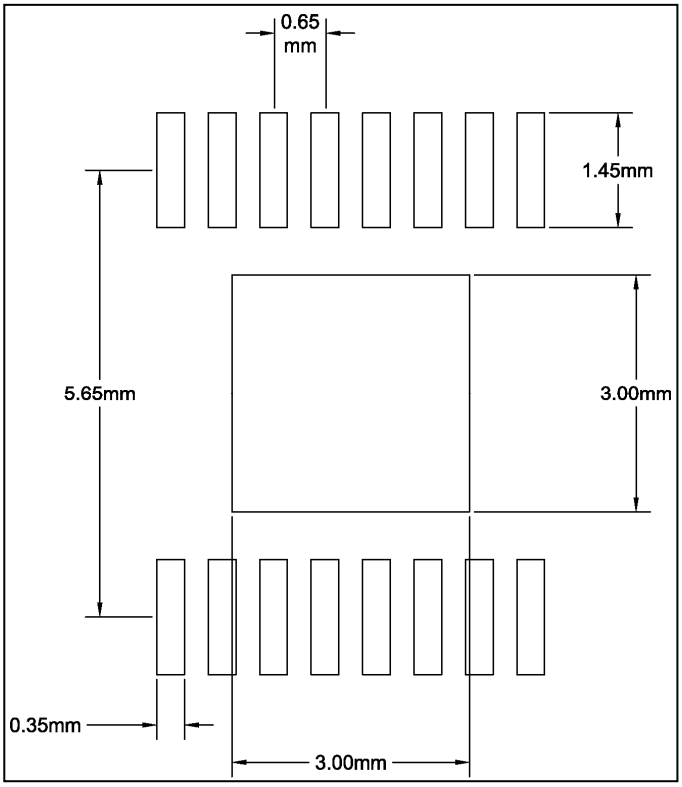
eTSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70		3.10
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50		3.10
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2017.09.09