IS37SML01G8A IS37SMW01G8A

IS38SML01G8A IS38SMW01G8A

IS37SML02G8A IS37SMW02G8A

IS38SML02G8A IS38SMW02G8A

IS37SML04G8A IS37SMW04G8A

IS38SML04G8A IS38SMW04G8A

IS37SML08G8A IS37SMW08G8A

IS38SML08G8A IS38SMW08G8A

1Gb/2Gb/4Gb/8Gb SPI NAND
133MHZ/104MHZ MULTI I/O INTERFACE

ADVANCED DATA SHEET

Long-term Support
World Class Quality

1Gb/2Gb/4Gb/8Gb, SPI NAND FLASH MEMORY
133MHz/104MHz MULTI I/O SPI INTERFACE with On-Chip ECC

ADVANCED INFORMATION

FEATURES

- **Single-level cell (SMC) technology**

- **Architecture**
  - Memory Cell: 1bit/Memory Cell
  - Page Size : 2176 bytes (2048 + 128) bytes
  - Block Size: 64 pages (128K + 8K) bytes
  - Plane Size: 1024 blocks per plane
  - Device Size:
    1Gb: 1 plane x 1024 blocks = 1024 blocks
    2Gb: 2 plane = 2048 blocks
    4Gb: 2 die x 2 plane = 4096 blocks
    8Gb: 4 die x 2 plane = 8192 blocks

- **Standard and extended SPI-compatible serial bus interface**
  - Instruction, address on 1 pin; data out on 1, 2,or 4 pins (1-1-1, 1-1-2 or 1-1-4)
  - Instruction on 1 pin; address, data out on 2,or 4 pins (1-2-2 or 1-4-4)
  - Instruction, address on 1 pin; data in on 1, or 4 pins (1-1-1 or 1-1-4)

- **User-selectable On Chip ECC**
  - 8 bit ECC per sector
  - The default state of On Chip ECC is enabled.

- **Array performance**
  - 133MHz clock frequency (MAX)
  - Page Read:
    25us (MAX) with On Chip ECC disabled
    70us (MAX) with On Chip ECC enabled
  - Page Program:
    300us (TYP) with On Chip ECC disabled
    320us (TYP) with On Chip ECC enabled
  - Erase Block: 2ms (TYP)

- **Operating Voltage Range & Speed**
  - 1.8V : V_{CC} = 1.7V ~1.95V, 104MHz max
  - 3.0V : V_{CC} = 2.7V ~3.6V, 133MHz max

- **Operating temperature**
  - Industrial: -40°C to +85°C
  - Automotive, A1: -40°C to +85°C
  - Automotive, A2: -40°C to +105°C

- **Device Initialization**
  - Automatic device initialization after power up

- **Advanced Features**
  - Read page cache mode
  - Read Unique ID
  - Read Parameter page

- **Security**
  - Blocks 7:0 are valid when shipped from factory with ECC enabled.
  - Software write protection with lock register
  - Hardware write protection to freeze BP bits
  - Lock tight to protect BP bits during one power cycle
  - Permanent block lock protection
  - OTP area: 30 pages one-time programmable (OTP) Flash memory area

- **Reliability**
  - Endurance: Typical 60K Program/Erase cycles with On Chip ECC enabled
  - Data Retention: 10 years

- **Industry Standard Pin-out & Packages**
  - H = 24-ball TFBGA 6x8x1.2 mm
  - I = 24-ball LFBGA 6x8x1.4 mm
  - J = 8-contact WSON 8x6mm
  - M = =16-pin SOIC 300mil

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non- volatile memory storage solution in systems where pin count must be kept to a minimum.

The ISSI IS37/38SML/SMW01G8A, IS37/38SML/SMW02G8A, IS37/38SML/SMW04G8A, and IS37/38SML/SMW-08G8A are 1Gb,2Gb, 4Gb and 8Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable On Chip ECC and first page auto-load on power up. With On Chip ECC enabled as the default after power on, ECC code is generated internally when a page is written to memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary.

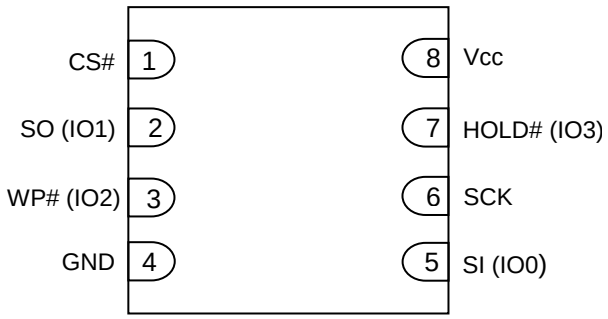
The On Chip 8-bit ECC logic is implemented in the device, which is enabled by default.

The On Chip ECC can be disabled or enabled again by command. When the On Chip 8-bit ECC logic is disabled, the host must handle the 8-bit ECC.

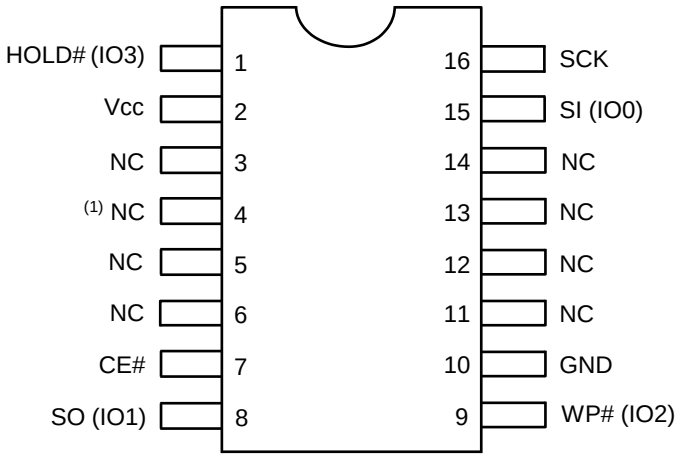
TABLE OF CONTENTS

1. PIN CONFIGURATION AND DESCRIPTION

8-contact WSON 8x6mm



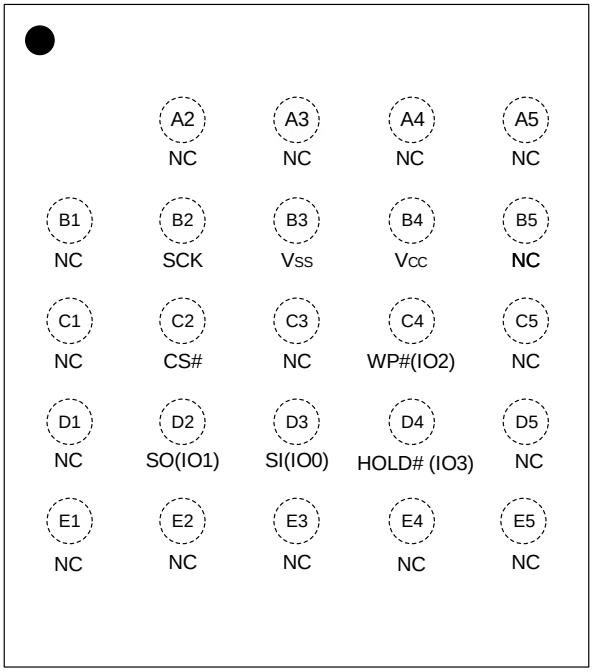
16-pin SOIC 300mil



Note:
1. DNU in 4Gb. DNU pin must be left in floating.

24-ball 5x5 ball array TFBGA/LFBGA

Top View, Balls Facing Down



Symbol	Type	Pin Function
CS#	Input	**Chip Select:** Places the device in active power mode when driven LOW. Deselects the device and places SO at HIGH-Z when HIGH. After power-up, the device requires a falling edge of CS# before any command can be written. This device goes into standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. In case of write-type instructions, CS# must be driven HIGH after a whole sequence is completed. Single command and address sequences and array-based operations are registered on CS#.
SCK	Input	**Serial Clock:** Provides serial interface timing. Latches commands, addresses, and data on SI on the rising edge of SCK. Triggers output on SO after the falling edge of SCK. While CS# is HIGH, keep SCK at Vcc or GND (determined by mode 0 or mode 3). Do not toggle SCK until CS# is driven LOW.
WP#	Input	**Write Protect:** When LOW, prevents overwriting block lock bits (BP [3:0] and TB) if the block register write disable (BRWD) bit is set. WP# must not be driven by the host during x4 READ operation. If the device is deselected, this pin defaults as an input pin**.**
HOLD#	Input	**Hold:** Hold function is disabled by default. When enabled, the external pull-up register is necessary to avoid accidental operation being placed on hold. Hold# pauses any serial communication with the device without deselecting it. To start HOLD condition, the device must be selected, with CS# driven LOW. During HOLD status (HOLD# driven LOW), SO is HIGH-Z and all inputs at SI and SCK are ignored. Hold mode starts at the falling edge of HOLD#, provided SCK is also LOW. If SCK is HIGH when HOLD# goes LOW, hold mode is kicked off at the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD#, provided SCK is also LOW. If SCK is HIGH, hold mode ends after the next falling edge of SCK. HOLD# must not be driven by the host during the x4 READ operation.
SI/IO0, SO/IO1, IO2, IO3	I/O	**Serial I/O:** The bidirectional I/O signals transfer address, data, and command information. If the device is deselected, IO [0, 2] defaults as an input pin and IO [1, 3] defaults as an output pin. SI must not be driven by the host during x2 or x4 READ operations.
VCC		**POWER:** VCC is the power supply for device.
VSS		**GROUND**
NC		**NO CONNECTION:** Not internal connection; can be driven or floated.
DNU		**Do Not Use:** DNUs must be left floating.

2. BLOCK DIAGRAM

The devices use an industry standard NAND Flash memory core organized by page/block with SPI interface.

The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. The modifications are specially to handle functions related to NAND Flash architecture. The interface supports page and random read/write and internal data move functions. The device also includes an On Chip ECC feature.
Data is transferred to or from the cell array, page-by-page, to a cache register and a data register. The cache register is closest to the I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array an acts as a data buffer for the Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. The cache register functions as the buffer memory to enable random data READ/WRITE operations. These devices also use a new SPI status register that reports the status of device operation.

Figure 2.1 Functional Block Diagram

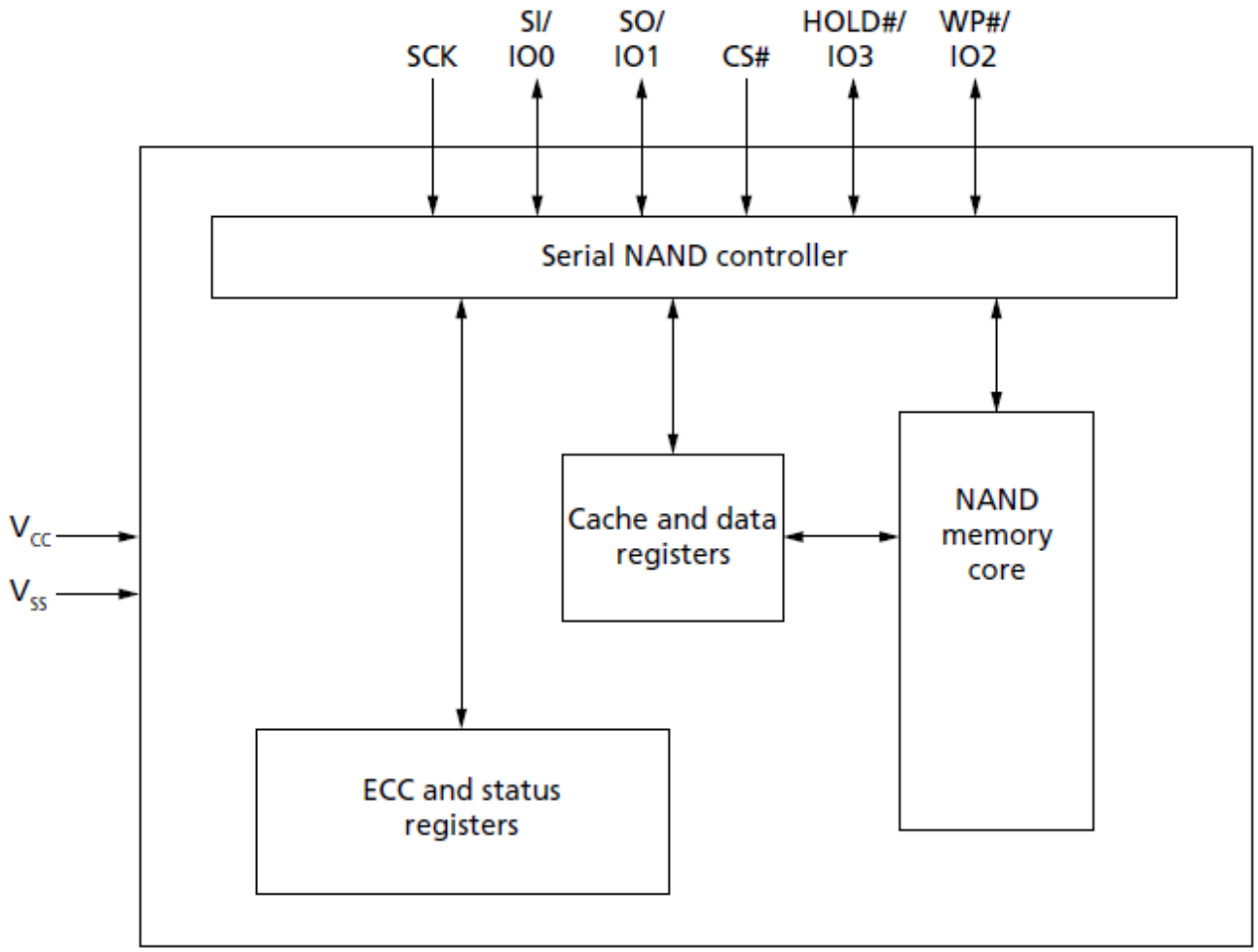
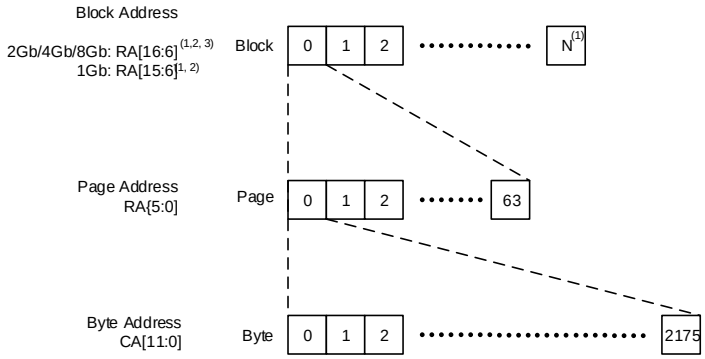


Figure 2.2 Memory Map



Notes:
1. N = 1023 for 1Gb, 2047 for 2Gb/4Gb/8Gb.
2. RA6 controls plane selection for 2Gb/4Gb/8Gb. No plane address for 1Gb.
3. Die selection in 4Gb/8Gb is set by Feature register setting (Address: D0h).

3. FEATURE OPERATIONS AND REGISTERS

3.1 GET FEATURES (0FH) AND SET FEATURES (1FH)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands either monitor the device status or alter the device configuration from the default at power-on. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP protect, block locking, SPI NOR like protocol configuration, and ECC correction can be managed by setting specific bits in feature addresses. Typically, the status register at feature address C0h is read to check the device status, except WEL, which is writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless specified otherwise, when the device is set, it remains set even if a RESET (FFh) command is issued. CFG [2:0] will be cleared to 000 after a reset and the device is back to normal operation.

Figure 3.1 GET FEATURES (0Fh) Timing

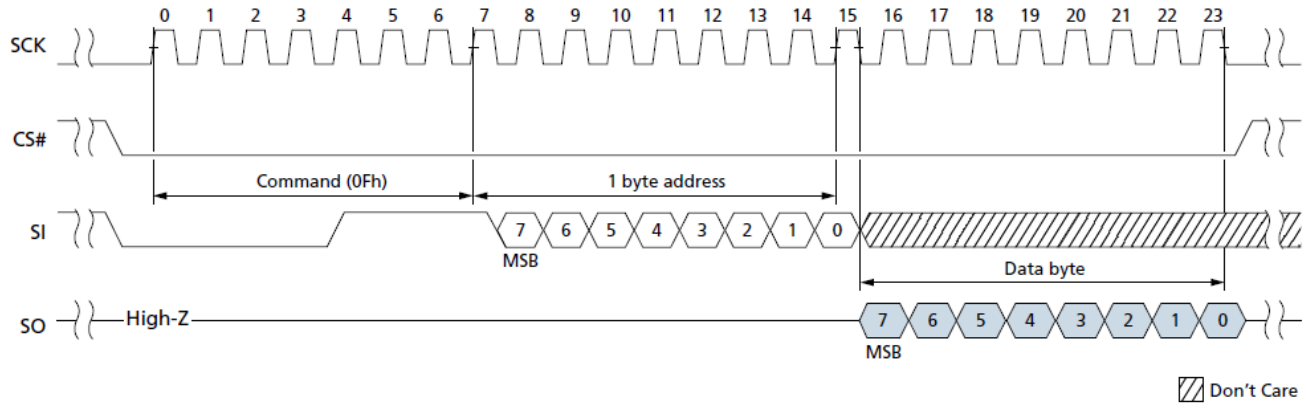
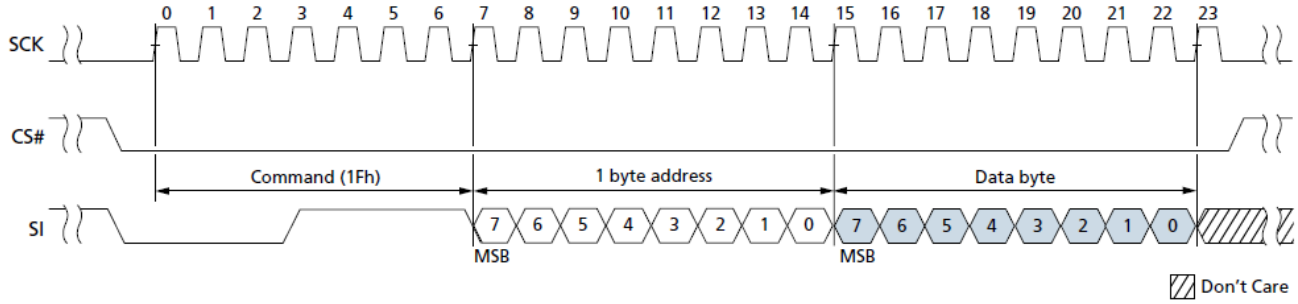


Figure 3.2 SET FEATURES (1Fh) Timing



1.1 FEATURE SETTINGS

Table 3.1 Feature Address Settings and Data Bits

Register		Feature Address	Feature Data Bits								Notes
			7	6	5	4	3	2	1	0	
Block lock		Address = A0h; Access = R/W	BRWD	BP3	BP2	BP1	BP0	TB	WP#/HOLD # Disable	-	1,2
Configuration		Address = B0h; Access = R/W	CFG2	CFG1	LOT_EN	ECC_EN	-	-	CFG0	-	1
Status		Address = C0h; Access = R	CRBSY	ECCS2	ECCS1	ECCS0	P_Fail	E_Fail	WEL	OIP	1
Die Select	4Gb	Address = D0h; Access = R/W	-	DS0	-	-	-	-	-	-	3
	8Gb		DS1	DS0	-	-	-	-	-	-	

Notes:
1. See the corresponding register bit description in Security Features, ECC Protection, Status Register, and Read Protocol – Similar to SPI NOR sections.
2. When the WP#/HOLD# disable bit is at the default value of 0, and with BRWD set to 1 and WP# LOW, block lock registers [7:2] cannot be changed.
3. Die Selects only available in 4Gb and 8Gb

3.1. DIE SELECTION

After power up or RESET, Die 0 is the default die selected in 4Gb and 8Gb. For example, the host can use the SET FEATURE command (1Fh) with D0h address and data 40h to select die 1. RESET and SET FEATURE commands are listened by both the die simultaneously. Do not use GET FEATURE command to detect device status during initialization or RESET. Wait 1.25mS after power up before issuing any command.

SET FEATURE is also not allowed when any LUN is in busy state to avoid two LUNs have different FEATURE register values (such as, both LUNs being selected). The rest of command sets are listened only by the selected die.

Table 3.2 DIE SELECTION (4Gb, 8Gb)

		Set Feature Command Address	Set Feature Command Data
4Gb	Die 0	D0h	0h
	Die 1		40h
8Gb	Die 0		0h
	Die 1		40h
	Die 2		80h
	Die 3		B0h

3.2. STATUS REGISTER

The device has an 8-bit status register that software can read during the device operation. All bits are read-only register except WEL, which could be changed by WRITE DISABLE (04h) and WRITE ENABLE (06h) commands. None of bits can be changed by SET FEATURE command (1Fh). The status register can be read by issuing the GET FEATURES (0Fh) command, followed by the feature address (C0h). The status register will output the status of the operation.

Table 3.3 Status Register Bit Definitions

Bit	Name	Description
7	Cache read busy (CRBSY)	This bit is set (CRBSY = 1) when READ PAGE CACHE RANDOM command is executing; this bit remains a 1 until the page specified at READ PAGE CACHE RANDOM command is transferred
6	ECC status register (ECCS2)	ECC status is set to 000b either following a RESET or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC status is invalid if ECC is disabled (via a SET FEATUREs command to get access the configuration register). After a power-up RESET, ECC status is set to reflect the contents of block 0, page 0.
5	ECC status register (ECCS1)	
4	ECC status register (ECCS0)	
3	Program fail (P_Fail)	Indicates that a program failure has occurred (P_FAIL = 1). This bit will also be set if the user attempts to program a locked or protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
2	Erase fail (E_Fail)	Indicates that an erase failure has occurred (E_FAIL = 1). This bit will also be set if the user attempts to erase a locked region or if the ERASE operation fails. This bit is cleared at the start of the BLOCK ERASE command sequence or a RESET command (E_FAIL = 0).
1	Write Enable Latch (WEL)	Indicates the current status of the write enable latch (WEL) and must be set to 1 prior to issuing a PROGRAM EXECUTE. This bit will also be set if the user attempts to erase a locked region or if the ERASE operation fails. This bit is cleared at the start of the BLOCK ERASE command sequence or a RESET command (E_FAIL = 0).
0	Operation In Progress (OIP)	This bit is set to 1 when a PROGRAM EXECUTE, PAGE READ, READ PAGE CACHE LAST, BLOCK ERASE, READ PAGE CACHE RANDOM (within tRCBSY to wait for cache register readness), RESET command, or a power-up initialization is executing; the device is busy. When the bit is 0, the interface is in the ready state.

3.3. SPI NOR READ CONFIGURATION

To be drop-in compatible to SPI NOR read protocol, the device offers an alternative solution to implement 03h/0Bh commands.

4. BUS OPERATION AND COMMAND DESCRIPTION

4.1 SPI MODE

The device can be driven by a host with its SPI running in either of two modes depending on clock polarity (CPOL) and clock phase (CPHA) settings:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

The difference between two modes is that the clock polarity when the bus matster is in standby mode and not transferring data.

- **SCK =0 for CPOL = 0, CPHA = 0 (Mode 0)**
- SCK =1 for CPOL = 1, CPHA = 1 (Mode 3)

4.2 SPI PROTOCOLS

Standard SPI: Command, address, and data are transmitted on a single data line (1-1-1 operation). Input on SI is latched in on the rising edge of SCK. Output on SO is available on the falling edge of SCK.

Extended SPI: An extension of the SPI protocol: 1-1-2, 1-1-4, 1-2-2, 1-4-4

- Command is transmitted on a single data line through SI.
- Addresses is transmitted on a single data line (SI), two, or four data lines, IO [3:0], depending on the command.
- Data is transmitted on two or four data lines, IO [3:0], depending on the command

4.3 SPI NAND COMMAND DEFINITIONS

Table 4.1 Command Set

Command	Op Code	Add. Bytes	Dummy Bytes	Data Bytes	Comments
Reset Operations					
RESET	FFh	0	0	0	Reset the device
Identification Operation					
READ ID	9Fh	0	1	2	Read Device ID
Feature Operation					
GET FEATURES	0Fh	1	0	1	Get features
SET FEATURES	1Fh	1	0	1	Set features
Read Operation					
PAGE READ	13h	3	0	0	Array read
READ PAGE CACHE RA-NDOM	30h	3	0	0	Cache read
READ PAGE CACHE LAST	3Fh	0	0	0	Ending of cache read
READ from CACHE x1	03h, 0Bh(1)	2	1	1 to 2176	Output cache data at column address
READ from CACHE x2	3Bh	2	1	1 to 2176	Output cache data on IO[1:0]
READ from CACHE x4	6Bh	2	1	1 to 2176	Output cache data on IO[3:0]
READ from CACHE Dual I/O	BBh	2	2	1 to 2176	Input Address/Output cache data on IO[1:0]
READ from CACHE Quad I/O	EBh	2	2	1 to 2176	Input Address/Output cache data on IO[3:0]
Write Enable/Disable Operation					
WRITE ENABLE	06h	0	0	0	Sets the WEL bit in the status register to 1
WRITE DISABLE	04h	0	0	0	Clears the WEL bit in the status register to 0
Erase Operation					
Block Erase	D8h	3	0	0	Block Erase
Program Operation					
PROGRAM EXECUTE	10h	3	0	0	Array program
PROGRAM LOAD x1	02h	2	0	1 to 2176	Load program data into cache register on SI
PROGRAM LOAD x4	32h	2	0	1 to 2176	Load program data into cache register on IO[3:0]
PROGRAM LOAD RANDOM DATA x1	84h	2	0	1 to 2176	Overwrite cache register with input data on SI
PROGRAM LOAD RANDOM DATA x4	34h	2	0	1 to 2176	Overwrite cache register with input data on IO [3:0]
PERMANENT BLOCK LOCK PROTECTION	2Ch	3	0	0	Permanently protect a specific group of blocks

Notes:
1. 03h and 0Bh command is the same at SPI NAND mode, but in SPI NOR mode, 03h is normal read without dummy, and 0Bh is fast read with dummy.

4.4 SERIAL INPUT AND OUTPUT TIMING

Figure 4.1 Serial Input Timing

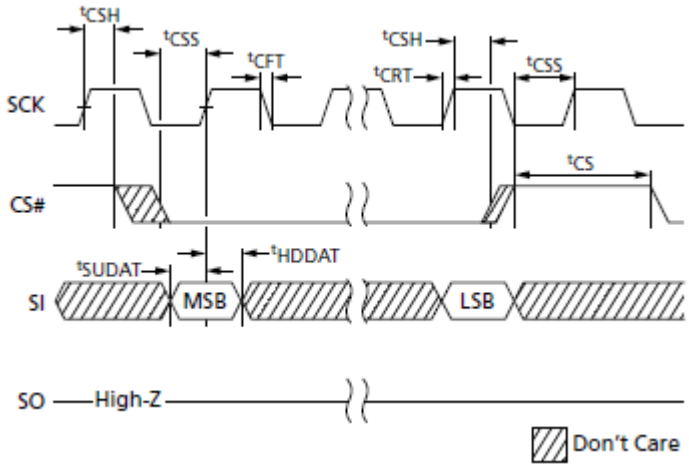


Figure 4.2 Serial Output Timing

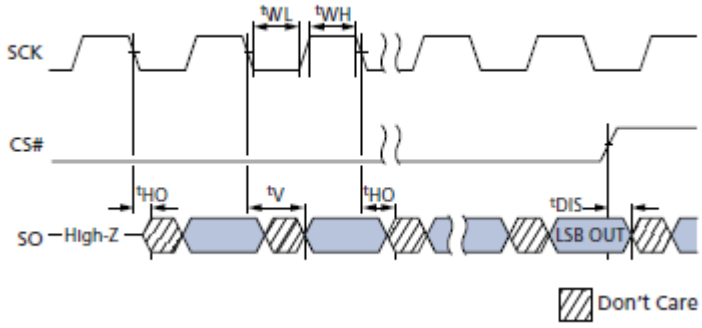
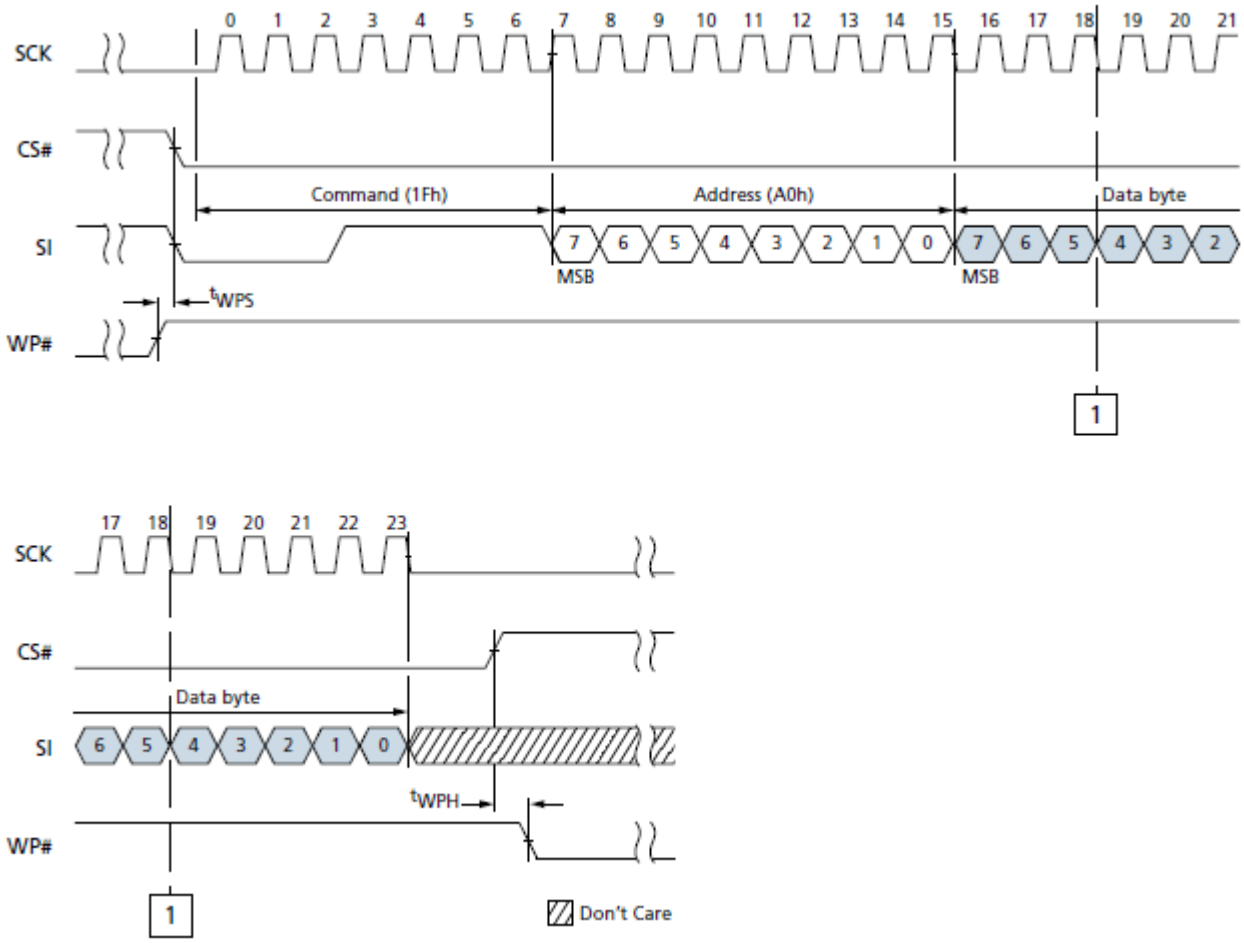


Figure 4.3 WP# Timing



5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS (1)

Voltage on any pin relative to Vss

Storage Temperature		-65°C to +150°C
Supply Voltage	3.0V device	-0.6V to +4.6V
	1.8V device	-0.6V to +2.4V
I/O Voltage	3.0V device	-0.6V to +4.6V
	1.8V device	-0.6V to +2.4V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

5.2 RECOMMENDED OPERATING CONDITIONS

Operating Temperature	Industrial Grade	-40°C to 85°C
	Automotive Grade A1	-40°C to 85°C
	Automotive Grade A2	-40°C to 105°C
V_{CC} Supply Voltage	3.0V device	2.7V (VMIN) – 3.6V (VMAX); 3.0V (Typ)
	1.8V device	1.7V (VMIN) – 1.95V (VMAX); 1.8V (Typ)

5.3 AC PIN CAPACITANCE (TA = 25°C, VCC= 3.0V/1.8V, 1MHZ)

			1Gb, 2Gb		4Gb		8Gb		Units
Symbol	**Parameter**	**Test Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
C_{IN}	Input Capacitance	V_{IN} = 0V	-	8	-	16	-	32	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	-	8	-	16	-	32	pF

Note:

1. These parameters are characterized and not 100% tested.

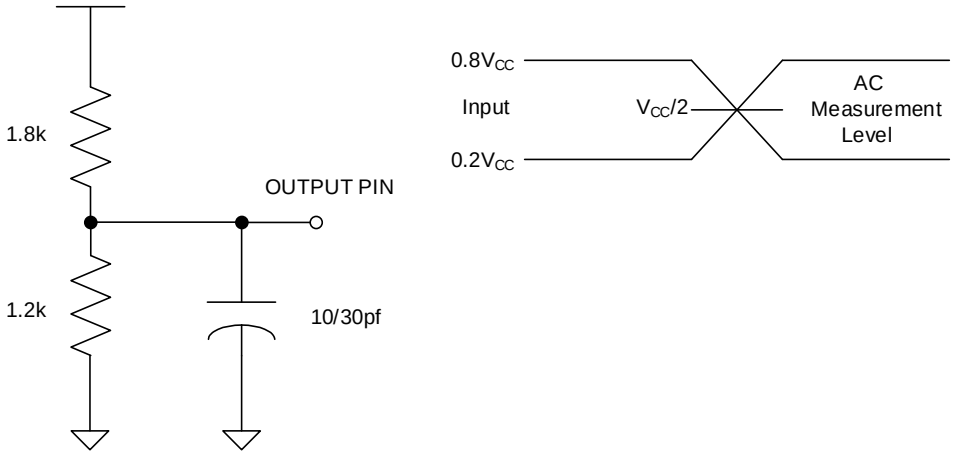
5.4 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 30/10		pF
TR,TF	Input Rise and Fall Times		5	ns
	Input Rise and Fall Times (>100MHz)		1.5	
VIN	Input Pulse Voltages(1)	0.2V_{CC}	0.8V_{CC}	V
VREFI	Input Timing Reference Voltages	0.3V_{CC}	0.7V_{CC}	
VREFO	Output Timing Reference Voltages	0.5V_{CC}		

Notes:

1. These are Min/Max specifications for dual/quad operations.

Figure 5.1 Output test load & AC measurement I/O Waveform



5.5 DC CHARACTERISTICS

Parameter		Symbol	Test Conditions		Min	Typ.	Max	Unit	Notes
Operating Current	Page Read	ICC3	-		-	37	47	mA	
	Program	ICC4	-		-	32	37		
	Erase	ICC5	-		-	32	37		
Stand-by Current (CMOS)		ICC1	$CE\#=V_{CC}$, $V_{IN}=V_{SS}$ or V_{CC}	1Gb, 2Gb	-	15	50	uA	
				4Gb		30	100		
				8Gb		60	200		
Input Leakage Current		ILI	-	1Gb, 2Gb	-	-	+/-10	uA	
				4Gb			+/-20		
				8Gb			+/-40		
Output Leakage Current		ILO	-	1Gb, 2Gb	-	-	+/-10	uA	
				4Gb			+/-20		
				8Gb			+/-40		
Input High Voltage		VIH	-		0.7xVCC	-	Vcc+0.4	V	
Input Low Voltage, All inputs		VIL	-		-0.5	-	0.3xVCC		
Output High Voltage Level		VOH	IOH=-100 uA		VCC-0.2	-	-		
Output Low Voltage Level		VOL	IOL=100 uA		-	-	0.2		

Notes:
1. Typical values are given for TA = 25°C
2. These parameters are verified in device characterization and are not 100% tested.

5.6 AC CHARACTERISTICS FOR ADDRESS/ COMMAND/DATA INPUT

3.0V

Parameter		Symbol	Min	Max	Unit	Notes
Clock frequency		tC	-	133	MHz	1, 2
Clock LOW time		tWL	3.375	-	ns	
Clock HIGH time		tWH	3.375	-	ns	
Clock LOW time (SPI NOR read 03h mode at 20MHz)		tWL	22.5	-	ns	
Clock HIGH time (SPI NOR read 03h mode at 20MHz)		tWH	22.5	-	ns	
Clock rise time		tCRT	1.3	-	V/ns	
Clock fall time		tCFT	1.3	-	V/ns	
Command deselect time		tCS	30	-	ns	
CE# Active setup/hold time relative to SCK		tCSS/tCSH	3.375	-	ns	
CE# Non-Active setup/hold time relative to SCK		tSHCH/tCHSL	2.5		ns	
Output disable time		tDIS	-	6	ns	
Data Input setup time		tSUDAT	2.5	-	ns	
Data Input hold time		tHDDAT	1.75	-	ns	
Clock LOW to output valid	30pF	tV	-	6	ns	1
	10pF		-	5	ns	
Clock LOW to output valid (similar to SPI NOR read 03h mode at 20MHz)	30pF		-	30	ns	
	10pF		-	28	ns	
Output hold time	30pF	tHO	2	-	ns	
	10pF		1.5	-	ns	
Output hold time (SPI NOR read 03h mode at 20MHz)	30pF	tHO	0	-	ns	
	10pF		0	-	ns	
WP# setup time		tWPS	20	-	ns	
WP# hold time		tWPH	100	-	ns	

Notes:

1. Read from Cache Dual I/O (BBh) and Quad I/O (EBh) can run up to 108MHz
2. When read protocol similar to SPI NOR mode is enabled, Read from Cache 03h command (no dummy) can run up to 20MHz, while read from Cache 0Bh command (8 dummy cycles) can run up to 133MHz.

1.8V

Parameter		Symbol	Min	Max	Unit	Notes
Clock frequency		tC	-	104	MHz	1, 2
Clock LOW time		tWL	4.5	-	ns	
Clock HIGH time		tWH	4.5	-	ns	
Clock LOW time (SPI NOR read 03h mode at 20MHz)		tWL	22.5	-	ns	
Clock HIGH time (SPI NOR read 03h mode at 20MHz)		tWH	22.5	-	ns	
Clock rise time		tCRT	1.3	-	V/ns	
Clock fall time		tCFT	1.3	-	V/ns	
Command deselect time		tCS	30	-	ns	
CE# Active setup/hold time relative to SCK		tCSS/tCSH	4.5	-	ns	
CE# Non-Active setup/hold time relative to SCK		tSHCH/tCHSL	3.5		ns	
Output disable time		tDIS	-	10	ns	
Data Input setup time		tSUDAT	3.0	-	ns	
Data Input hold time		tHDDAT	2.0	-	ns	
Clock LOW to output valid	30pF	tV	-	7	ns	1
	10pF		-	6	ns	
Clock LOW to output valid (similar to SPI NOR read 03h mode at 20MHz)	30pF		-	30	ns	
	10pF		-	28	ns	
Output hold time	30pF	tHO	2.5	-	ns	
	10pF		2.0	-	ns	
Output hold time (SPI NOR read 03h mode at 20MHz)	30pF	tHO	0	-	ns	
	10pF		0	-	ns	
WP# setup time		tWPS	20	-	ns	
WP# hold time		tWPH	100	-	ns	

Notes:

1. Read from Cache Dual I/O (BBh) and Quad I/O (EBh) can run up to 80MHz
2. When read protocol similar to SPI NOR mode is enabled, Read from Cache 03h command (no dummy) can run up to 20MHz, while read from Cache 0Bh command (8 dummy cycles) can run up to 104MHz.

5.7 PROGRAM/READ/ERASE CHARACTERISTICS

Parameter		Symbol	Typ	Max	Unit	Notes
BLOCK ERASE operation time (128KB)		tERS	2	10	ms	
PROGRAM PAGE operation time	On Chip ECC disabled	tPROG	300	700	us	
	On Chip ECC enabled		320	700		
Page read time	On Chip ECC disabled	tRD	-	25	us	
	On Chip ECC enabled		45	70		
Data transfer time from data register to cache register	On Chip ECC disabled	tRCBSY	-	5	us	
	On Chip ECC enabled		40	50		
Power-on reset time (Device initialization) from Vcc Min		tPOR	-	1.25	ms	
Write inhibit voltage	3.0V	V_{WI}	-	2.5	V	
	1.8V			1.5		
Reset time for READ, PROGRAM, and ERASE operations	On Chip ECC disabled	tRST	-	30/35/525	us	1
	On Chip ECC enabled		-	75/80/570		
Number of partial-page programming operations		NOP	-	4	-	2

Notes:

1. For power-up RESET operation, tRST will be tPOR of 1.25ms maximum. For stacked die (4Gb, 8Gb), no GET FEATURE command should be issued during this time of tRST.
2. In the main user area and in user meta data area I, single partial-page programming operations must be used. Within a page, the user can perform a maximum of four partial page programming operations.

6. Security

6.1 VOLATILE BLOCK PROTECTION

The block lock feature protects the entire device or ranges of device blocks from the PROGRAM and ERASE operations. The SET FEATURE command must be issued to alter the state of block protection. After power-up, the device is in the locked state by default; **block protection register bits BP [3:0] and TB are 1**. **Reset will not modify the block protection state.** When a PROGRAM/ERASE command is issued to a locked block, a status register P_Fail bit or E_Fail bit will be set to indicate the operation failure.

The following command sequence unlocks all blocks after power-up:

- SET FEATURES REGISTER WRITE (1Fh) + feature address (A0h) + 00h on data bits.

The command sequence typically consists of a COMMAND LATCH cycle, address input cycles, and one or more data cycles, either READ or WRITE.

Table 6.1 Block Lock Register Block Protect Bits

TB	BP3	BP2	BP1	BP0	Protected Portion	Protected Blocks			
						1Gb	2Gb	4Gb	8Gb
0	0	0	0	0	None – all unlocked	None			
0	0	0	0	1	Upper 1/1024 locked	1023	2046:2047	4092:4095	8184:8191
0	0	0	1	0	Upper 1/512 locked	1022:1023	2044:2047	4088:4095	8176:8191
0	0	0	1	1	Upper 1/256 locked	1020:1023	2040:2047	4080:4095	8160:8191
0	0	1	0	0	Upper 1/128 locked	1016:1023	2032:2047	4064:4095	8128:8191
0	0	1	0	1	Upper 1/64 locked	1008:1023	2016:2047	4032:4095	8064:8191
0	0	1	1	0	Upper 1/32 locked	992:1023	1984:2047	3968:4095	7936:8191
0	0	1	1	1	Upper 1/16 locked	960:1023	1920:2047	3840:4095	7680:8191
0	1	0	0	0	Upper 1/8 locked	896:1023	1792:2047	3584:4095	7168:8191
0	1	0	0	1	Upper 1/4 locked	768:1023	1536:2047	3072:4095	6144:8191
0	1	0	1	0	Upper 1/2 locked	512:1023	1024:2047	2048:4095	4096:8191
0	1	All others			All locked	0:1023	1024:2047	0:4095	0:8191
1	0	0	0	0	None – all unlocked	None			
1	0	0	0	1	Lower 1/1024 locked	0	0:1	0:3	0:7
1	0	0	1	0	Lower 1/512 locked	0:1	0:3	0:7	0:15
1	0	0	1	1	Lower 1/256 locked	0:3	0:7	0:15	0:31
1	0	1	0	0	Lower 1/128 locked	0:7	0:15	0:31	0:63
1	0	1	0	1	Lower 1/64 locked	0:15	0:31	0:63	0:127
1	0	1	1	0	Lower 1/32 locked	0:31	0:63	0:127	0:255
1	0	1	1	1	Lower 1/16 locked	0:63	0:127	0:255	0:511
1	1	0	0	0	Lower 1/8 locked	0:127	0:255	0:511	0:1023
1	1	0	0	1	Lower 1/4 locked	0:255	0:511	0:1023	0:2047
1	1	0	1	0	Lower 1/2 locked	0:511	0:1023	0:2047	0:4095
1	1	All others			All locked	0:1023	0:2047	0:4095	0:8191
1	1	1	1	1	All locked (default)	0:1023	0:2047	0:4095	0:8191

6.2 HARDWARE WRITE PROTECTION

Hardware write protection prevents the block protection state from hardware modifications.

In order to utilize this feature, SET FEATURE command is issued on the feature address A0h and WP#/HOLD# disable bit state is set to 0.

The BRWD bit is operated in conjunction with WP#/HOLD# disable bit. When BRWD is set to 1 and WP# is LOW, none of the other block register bits [7:2] can be set. The block lock state cannot be changed, regardless of what is unlocked or locked. Also, when the WP#/HOLD# disable bit is set to 1, the hardware protected mode is disabled. The default value of BRWD and WP#/HOLD# disable bits = 0 after power up.

6.3 DEVICE LOCK TIGHT (LOT)

The LOCK TIGHT mode prevents the block protection state from software modifications. After it is enabled, this mode cannot be disabled by a software command. Also, BP, TB, and BRWD bits are protected from further software changes. **Only another power cycle can disable the LOCK TIGHT mode.**

- SET FEATURES REGISTER WRITE (1Fh) + feature address (B0h) + data bit set to enable LOT (LOT_EN bit = 1).

When the hardware write protection mode is disabled during quad or x4 mode, LOCK TIGHT can be used to prevent a block protection state change.

6.4 PERMANENT BLOCK LOCK PROTECTION

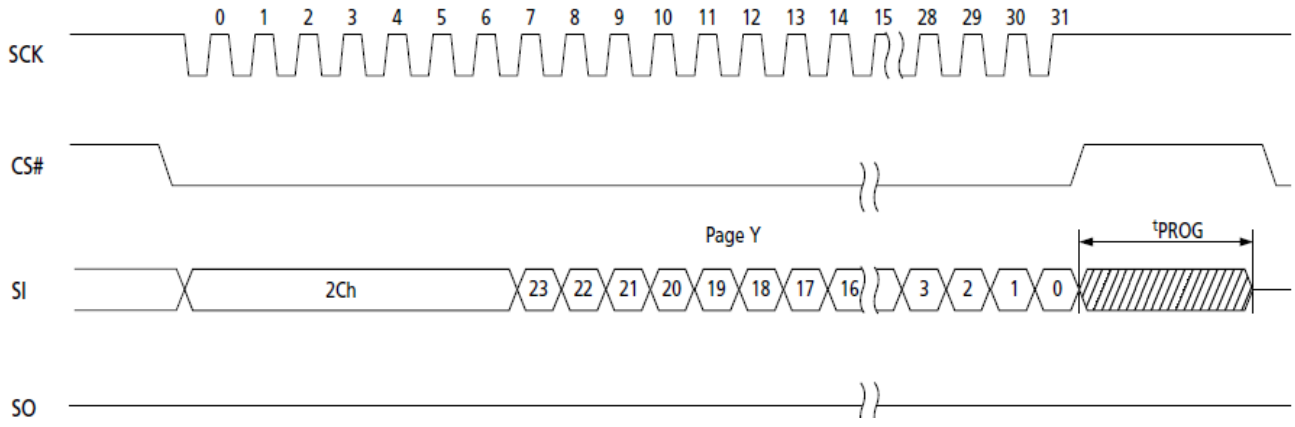
Twelve groups of blocks per die can be permanently locked using PROTECT command. The PROTECT command provides nonvolatile, irreversible protection of up to twelve groups (24 blocks in 1Gb, 48 blocks in 2Gb/4Gb/8Gb). Implementation of the protection is group-based, which means that a minimum of one group (2 blocks in 1Gb, 4 blocks in 2Gb/4Gb/8Gb) is protected when PROTECT command is issued.

The device is shipped from the factory with no blocks protected so that users can program or erase the blocks before issuing the PROTECT command. Block protection is also irreversible in that when protection is enabled by issuing the PROTECT command, the protected blocks can no longer be programmed or erased. If PERMANENT LOCK is disabled, PROTECT command would be ignored. As with any command that changes the memory contents, the WRITE ENABLE must be executed. If this command is not issued, then the protection command is ignored. WRITE ENABLE must be followed by a PROTECTION command (2Ch)

PROTECT SEQUENCE

- 06h (WRITE ENABLE)
- 2Ch (PERMANENT BLOCK LOCK PROTECTION)
- 24-bit address
- After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P_FAIL bit.

Figure 6.1 PROTECT command Cycle



PERMANENT BLOCK LOCK PROTECTION COMMAND (2Ch) Details

To enable protection, the PROTECTION command consists of an 8-bit command code (2Ch), followed by a 24-bit address (8 dummy bits +16-bit valid page block address in 1Gb, 7 dummy bits +17-bit valid page block address in 2Gb/4Gb/8Gb). Row address bits 11, 10, 9, 8 (named as Y) input the targeted block group information. When Y defines the group of blocks to be protected. There are 12 Groups Y where Y= 0000b – 1011b.

- Y=0000 protect Group 0 = block 0, 1, 2, 3.
- Y=0001 protect Group 1 = block 5, 6, 7, 8.
- ….
- Y=1011 protect Group 11 = block 44, 45, 46, 47.

After tPROG, the targeted block groups are protected. Upon PROTECT operation failure, the status register reports a value of 0Ch (P_FAIL = 1 and WEL = 1). Upon PROTECT operation success, the status register reports a value of 00h.

Note: There is no status register to check the PROTECT status of a block or a group. A permanent blocks table should be maintained and updated after a group is protected.

Permanent Block Lock Protection Disable Mode

This mode disables the ability to accept the PROTECTION command. Running this command sequence ensures no more groups can ever be permanently locked.

- SET FEATURE command (1Fh) with B0h mode and data value C2h.
- 06h (WRITE ENABLE).
- 10h (Excute with block/page address as “0”)
- After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P_Fail bit

6.5 ONE TIME PROGRAMMABLE (OTP)

This device offers a protected, one-time programmable memory area. Thirty full pages per die are available, and the entire range is guaranteed. Customers can choose how to use the OTP area, such as programming serial numbers or other data for permanent storage. The OTP area can't be erased.

When ECC is enabled, data written in the OTP area is ECC protected.

ENABLE OTP Access.

OTP access needs to be enabled in order to read and write to the OTP region. When the die is in OTP operation mode, all subsequent page program or page read commands are applied to the OTP area. SET FEATURES command (1Fh) with feature address B0h and data 50h (OTP operation mode with ECC enabled) or 40h (OTP operation mode with ECC disabled) are used to enable the OTP access.

After OTP access is enabled, the following sequence is used to program one or more pages

- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with the row address of page (OTP page address range 02h-0Bh)
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- Using GET FEATURE command (0Fh) with feature address C0h to verify P_FAIL bit is 0 for the successful operation.

After OTP access is enabled, the following sequence is used to read one or more pages

- PAGE READ command (13h) with the page address (02h-0Bh)
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- Page data using READ FROM CACHE command (03h).

OTP Configuration States

To check the status of OTP data protect, SPI NOR read enable, or PERMANENT BLOCK LOCK protection, the following sequence is used.

- SET FEATURES command (1Fh) with feature address B0h and data (C0h for OTP data protection bit, 82h for NOR read protocol enable bit, C2h for permanent block lock disable bit)
- PAGE READ command (13h) with address 0
- Verify until OIP bit not busy using GET FEATURE command (0Fh) with feature address C0h
- READ FROM CACHE command (03h) with address 0
- Expect the read from cache data all 1 for the mode disabled or all "0" for enabled

NOTE: Configuration status of CFG[2:0] can be read using FET FEATURE command (0Fh) with feature address B0h.

OTP Protection and Program Prevention

This mode is used to prevent further programming of the pages in the OTP area. To protect and prevent programming the OTP area, following sequence is used.

- SET FEATURES command (1Fh) with feature address B0h and data C0h (CFG [2:0]=110b.
- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with the row address 00h
- Verify until OIP bit not busy and P_FAIL bit 0 using GET FEATURE command (0Fh) with status register address C0h.

EXIT OTP

To exit OTP operation mode and return to normal array operation mode, following sequence is used.

- SET FEATURES command (1Fh) with feature address B0h and data CFG [2:0]=000b
- RESET (FFh) command

Table 6.2 Configuration Registers for Security

CFG2	CFG1	CFG0	State
0	0	0	Normal operation
0	1	0	Access OTP area/Parameter/Unique ID
1	1	0	Access to OTP data protection bit to lock OTP area
1	0	1	Access to SPI NOR read protocol enable mode
1	1	1	Access to permanent block lock protection disable mode

7. IDENTIFIVATION OPERATIONS

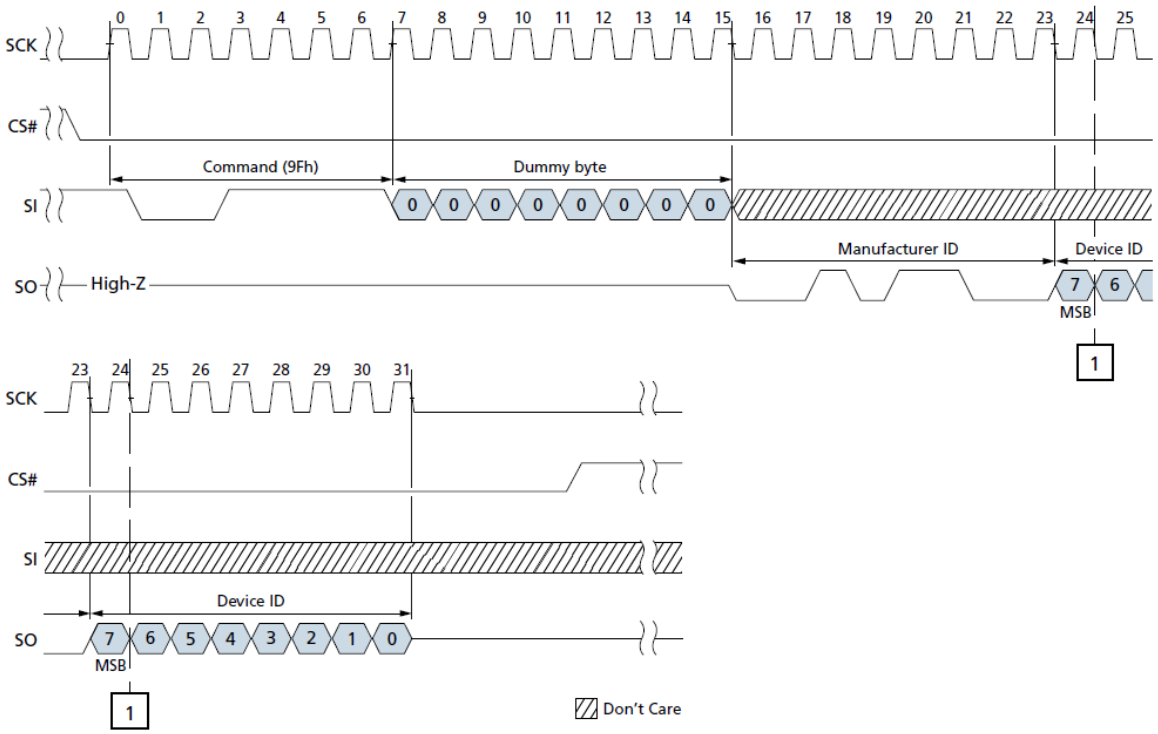
7.1 READ ID

READ ID reads the 2-byte identifier code programmed into the device, which includes ID and device configuration data as shown in the table below.

Table 7.1 READ ID Table

Byte	Description	7	6	5	4	3	2	1	0	Value
Byte 0	Manufacturer ID	1	0	0	1	1	1	0	1	9Dh
Byte 1	1Gb 3.0V Device ID	0	0	0	1	0	1	1	0	16h
Byte 1	1Gb 1.8V Device ID	0	0	0	1	0	1	1	1	17h
Byte 1	2Gb 3.0V Device ID	0	0	1	0	0	1	1	0	26h
Byte 1	2Gb 1.8V Device ID	0	0	1	0	0	1	1	1	27h
Byte 1	4Gb 3.0V Device ID	0	0	1	1	0	1	1	0	36h
Byte 1	4Gb 1.8V Device ID	0	0	1	1	0	1	1	1	37h
Byte 1	8Gb 3.0V Device ID	0	1	0	0	0	1	1	0	46h
Byte 1	8Gb 1.8V Device ID	0	1	0	0	0	1	1	1	47h

Figure 7.1 READ ID (9Fh) Timing



7.2 PARAMETER PAGE

The following command flow must be issued by the memory controller to access the parameter page:

1. 1Fh - SET FEATURES command with a feature address of **B0h** and data value for **CFG [2:0] = 010b** to access OTP/Parameter/Unique ID pages.
2. 13h - PAGE READ command with a block/page address of **0x01h**, and then check the status of the read completion using GET FEATURES (0Fh) command with a feature address of C0h.
3. 03h - READ FROM CACHE COMMAND with an address of **0x00h** to read the data out of the NAND device
4. 1Fh – SET FEATURES command with a feature address of **B0h** and data value for **CFG [2:0] = 000b** to exit the parameter page reading.

7.3 PARAMETER PAGE DATA STRUCTURE

Table 7.3 Parameter Page Data Structure

Revision Information and Feature Block				
Byte	**Description**			**Value**
0-3	Parameter page signature			4Fh, 4Eh, 46h, 49h
4-5	Revision number			00h (N/A)
6-7	Features supported			00h (N/A)
8-9	Optional commands supported			06h, 00h
10-31	Reserved			00h
Manufacturer Information Block				
32-43	Device manufacturer (12 ASCII characteristics)			49h, 53h, 53h, 49h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device Model	1Gb, 3.0V	IS37SML01G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 6Ch, 30h, 31h, 47h, 30h, 38h, 41hh, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		1Gb, 1.8V	IS37SMW01G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 57h, 30h, 31h, 47h, 30h, 38h, 41hh, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		2Gb, 3.0V	IS37SML02G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 6Ch, 30h, 32h, 47h, 30h, 38h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		2Gb, 1.8V	IS37SMW02G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 57h, 30h, 32h, 47h, 30h, 38h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		4Gb, 3.0V	IS37SML04G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 6Ch, 30h, 34h, 47h, 30h, 38h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		4Gb, 1.8V	IS37SMW04G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 57h, 30h, 34h, 47h, 30h, 38h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		8Gb, 3.0V	IS37SML08G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 6Ch, 30h, 38h, 47h, 30h, 38h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		8Gb, 1.8V	IS37SMW08G08A	49h, 53h, 33h, 37h, 53h, 6Dh, 57h, 30h, 38h, 47h, 30h, 38h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID			9Dh
65-66	Date Code			00h
67-79	Reserved			00h
Memory Organization				
Byte	**Description**			**Value**
80-83	Number of Data Bytes per Page			00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page			80h, 00h
86-89	Number of Data Bytes per Partial Page			00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page			20h, 00h
92-95	Number of Pages per Block			40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		1Gb	00h, 02h, 00h, 00h
			2Gb	00h, 04h, 00h, 00h
			4Gb	00h, 08h, 00h, 00h
			8Gb	00h, 0Ch, 00h, 00h
100	Number of logical units		1Gb	01h
			2Gb	01h
			4Gb	02h
			8Gb	04h

101	Number of address cycles (NA)		00h (N/A)
102	Number of bits per cell		01h
103-104	Bad blocks maximum per unit	1Gb	14h, 00h
		2Gb	28h, 00h
		4Gb	50h, 00h
		8Gb	A0h, 00h
105-106	Block Endurance		06h, 04h
107	Guaranteed Valid Blocks at Beginning of Target		01h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of program per page		04h
111	Partial programming attributes		00h
112	Number of ECC bits		00h
113	Number of interleaved address bits		00h (N/A)
114	Interleaved operation attributes		00h (N/A)
115-127	Reserved		00h
Electrical Parameters Block			
Byte	**Description**		**Value**
128	I/O pin capacitance	1Gb:8pF	08h
		2Gb:8pF	08h
		4Gb :16pF	10h
		8Gb :32pF	20h
129-130	Timing mode support		00h, 00h
131-132	Program cache timing mode support		00h, 00h
133-134	tPROG (MAX) page program time (uS)	700us	EEh, 02h
135-136	tERS (MAX) block erase time (uS)	10000us	10h, 27h
137-138	tR_ECC (MAX) page read time (uS)	70us	46h, 00h
139-140	tCCS Minimum change column setup time		00h (N/A)
141-163	Reserved		00h
Vendor Blocks			
Byte	**Description**		**Value**
164-165	Vendor-specific revision number (NA)		00h, 00h
166-179	Vendor-specific		00h
180-247	Reserved		00h
248	ECC maximum correct ability		08h
249-253	Reserved		00h
254-255	Integrity CRC (1)		Set at Test

Redundant Parameter Pages		
Byte	**Description**	**Value**
256-511	2nd copy of the parameter table	
512-767	3rd copy of the parameter table	
768+	Additional redundant parameter pages	

Note:

1. The integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC shall be calculated using the following 16-bit generator polynomial: G(X) = X16 + X15 + X2 + 1

7.4 UNIQUE ID PAGE

The following command flow must be issued by the memory controller to access the unique ID page contained within the device:

1. 1Fh - SET FEATURES command with a feature address of B0h and data value for 40h (to access OTP/Parameter/Unique ID pages/ECC Disable).
2. 13h - PAGE READ command with a block/page address of 0x00h, and then poll the status register OIP bit until device is ready using GET FEATURES (0Fh) command with a feature address of C0h.
3. 03h - READ FROM CACHE COMMAND with an address of 0x00h to read the Unique ID data out of the NAND device
4. 1Fh – SET FEATURES command with a feature address of B0h and data value of 10h or 00h (main array READ, ECC enable/disable) to exit Unique ID reading.

The device stores 16 copies of the Unique ID data. Each copy is 32 bytes: the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes.

The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, that copy of Unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the Unique ID data.

8. DEVICE OPERATION

8.1 POWER-UP SEQUENCE

POWER UP Sequence

At power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on Vcc. until Vcc reaches the correct values of Vcc, min at power-up (Adding a simple pull-up resistor on CE# is recommended.)

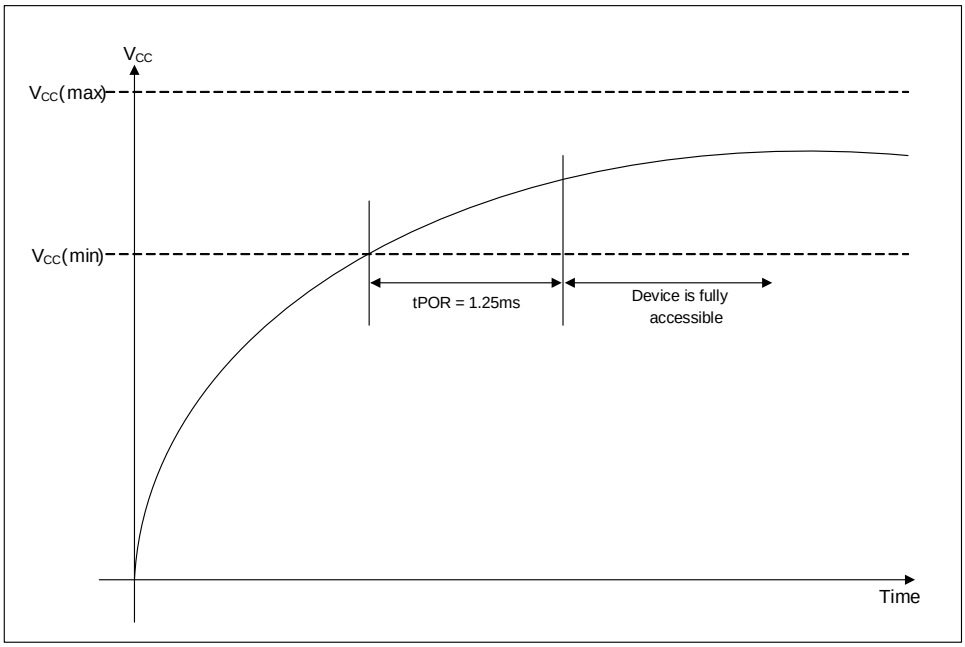
After the device reaches the power on level (Vcc, min), the internal initialization sequence will be triggered. At default setting, first page data would be automatically loaded into cache register during initialization period.

During the initialization period, GET FEATURE command could be issued to poll the status register (OIP) before first access (1Gb, 2Gb) except for stacked devices (4Gb, 8Gb). No other external command is accepted during initialization period of tPOR.

The device can be fully accessible tPOR (1.25ms) after VCC reaches the power-on level (Vcc, min).

During the power on and power off sequence, it is necessary to keep the WP#=LOW for the internal data protection.

Figure 8.1 Power-Up Sequence



Note: Poll status register OIP bit is allowed for 1Gb/2Gb during device initialization.

8.2 RESET

The RESET command (FFh) is used to put the memory into a known condition and to abort the command sequence in progress. READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. Once the RESET command is issued to the device, it will take tRST to complete reset operation.

During this period, the GET FEATURE command can be issued to monitor the status (OIP) except for the stacked devices (4Gb/8Gb). While the device is busy after sending RESET command, READ ID command can be issued to read device ID. For the stacked devices (4Gb/8Gb), no command should be issued until tRST. The first page of data of block 0 is auto-loaded to the cache register. For stacked device, Die 0 is selected as default and the first page of block 0 is loaded to the cache.

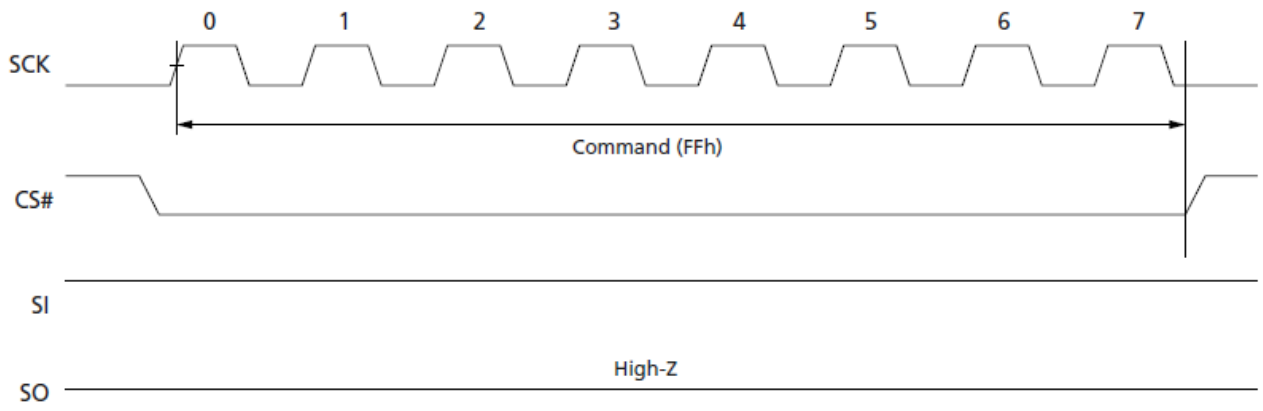
All other status register bits are cleared. The ECC status register bits will be updated after a reset.

The configuration register bits CFG [2:0] will be cleared after a reset.

All other configuration register bits will not be reset.

The block lock register bits will not be cleared after reset. **The block lock register bits will be cleared by POWER CYCLE or writing SET FEATURE command.**

Figure 8.2 RESET (FFh) Timing



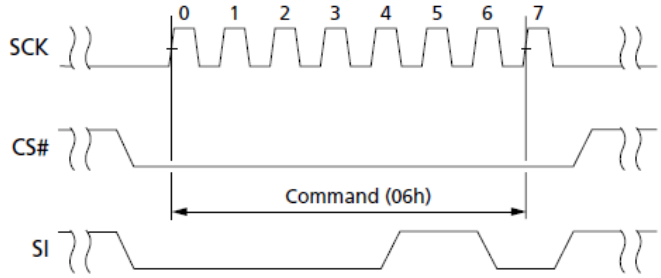
8.3 WRITE OPERATIONS

WRITE ENABLE (06h)

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. WRITE ENABLE is required in the following operations that change the contents of the memory array:

- **PAGE PROGRAM**
- **OTP AREA PROGRAM**
- **BLOCK ERASE**

Figure 8.3 WRITE ENABLE (06h) Timing

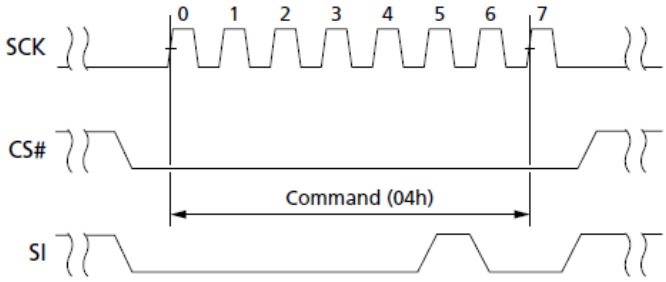


WRITE DISABLE (04h)

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0. Disabling the following operations:

- **PAGE PROGRAM**
- **OTP AREA PROGRAM**
- **BLOCK ERASE**

Figure 8.4 WRITE DISABLE (04h) Timing



8.4 ADDRESS REQUIREMENT

The device requires 24 bit address or 16 bit address for read, program, erase, and protection operations.

Command requires 24 bit address: PAGE READ (13h), READ PAGE CACHE RANDOM (30h), PROGRAM EXECUTE (10h), BLOCK ERASE (D8h), PERMANENT BLOCK LOCK PROTECTION (2Ch)

Command requires 16 bit address: READ FROM CACHE x1 (03h/0Bh), READ FROM CACHE x2 (3Bh), READ FROM CACHE x4 (6Bh), READ FROM CACHE DUAL I/O (BBh), READ FROM CACHE QUAD I/O EBh), PROGRAM LOAD x1 (02h), PROGRAM LOAD x4 (32h), PROGRAM LOAD RANDOM DATA x1 (84h), PROGRAM LOAD RANDOM DATA x4 (34h)

- **24 bit address is consist of dummy bits + valid block/page address like table 8.1.**

Table 8.1 24 bit Address Table

Density	Dummy bits	Valid block/page Address	Total (bit)
1Gb	8	RA[15:6] , 16 address	24
2Gb/4Gb/8Gb	7	RA[16:6], 17 address	24

- **16 bit address is consist of dummy bits + Plane select bit +12 column address or dummy bits + select bit +12 column address like table 8.2.**

Table 8.2 16 bit Address Table

Density	Dummy Bits (1)	Plane Select bit	Column Address	Total (bit)
1Gb	4	No	CA[11:0] , 12 address	16
2Gb/4Gb/8Gb	3	1 bit		16

Note: 1. "LOW" for dummy bits.

NOTE: Read from Cache (03h) in SPI NOR mode, and Fast Read from Cache (0Bh) in SPI NOR mode also requires 24 bit address, but it is consist of dummy bits + Column address.

Table 8.3 24 bit SPI NOR Mode Address Table

Density	Dummy Bits	Plane Select bit	Column Address	Total (bit)
1Gb	12	No	CA[11:0] , 12 address	24
2Gb/4Gb/8Gb	11	1 bit		24

8.5 PAGE READ OPERATION

The PAGE READ (13h) command transfers data from the cell array to the cache register. It requires a 24-bit address (dummy bits + valid block/page address).

After the 24-bit address is registered, the device starts the transfer from main array to the cache register. During this data transfer busy time of tRD, the GET FEATURES command can be issued to monitor the operation.

Following successful completion of PAGE READ, the READ FROM CACHE command must be issued to read data out of cache. The command sequence is as follows to transfer data from array to output:

13h (PAGE READ command to cache)

0Fh (GET FEATURES command to read the status)

03h or 0Bh (READ FROM CACHE): 1-1-1 READ

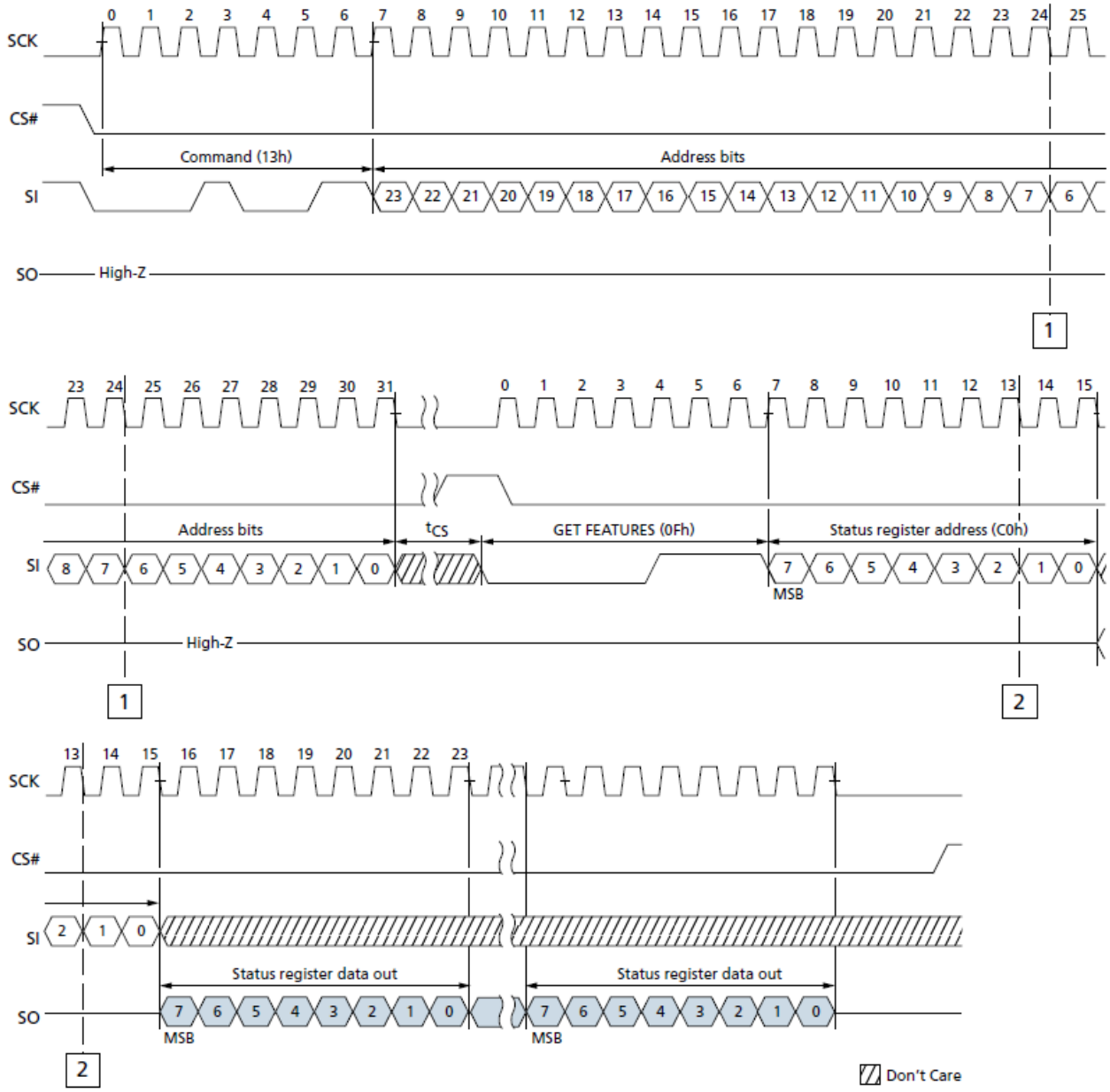
3Bh (READ FROM CACHE x2): 1-1-2 READ

6Bh (READ FROM CACHE x4): 1-1-4 READ

BBh (READ FROM CACHE DUAL I/O): 1-2-2 READ

EBh (READ FROM CACHE QUAD I/O): 1-4-4 READ

Figure 8.5 PAGE READ (13h) and GET FEATURES (0Fh) Timing

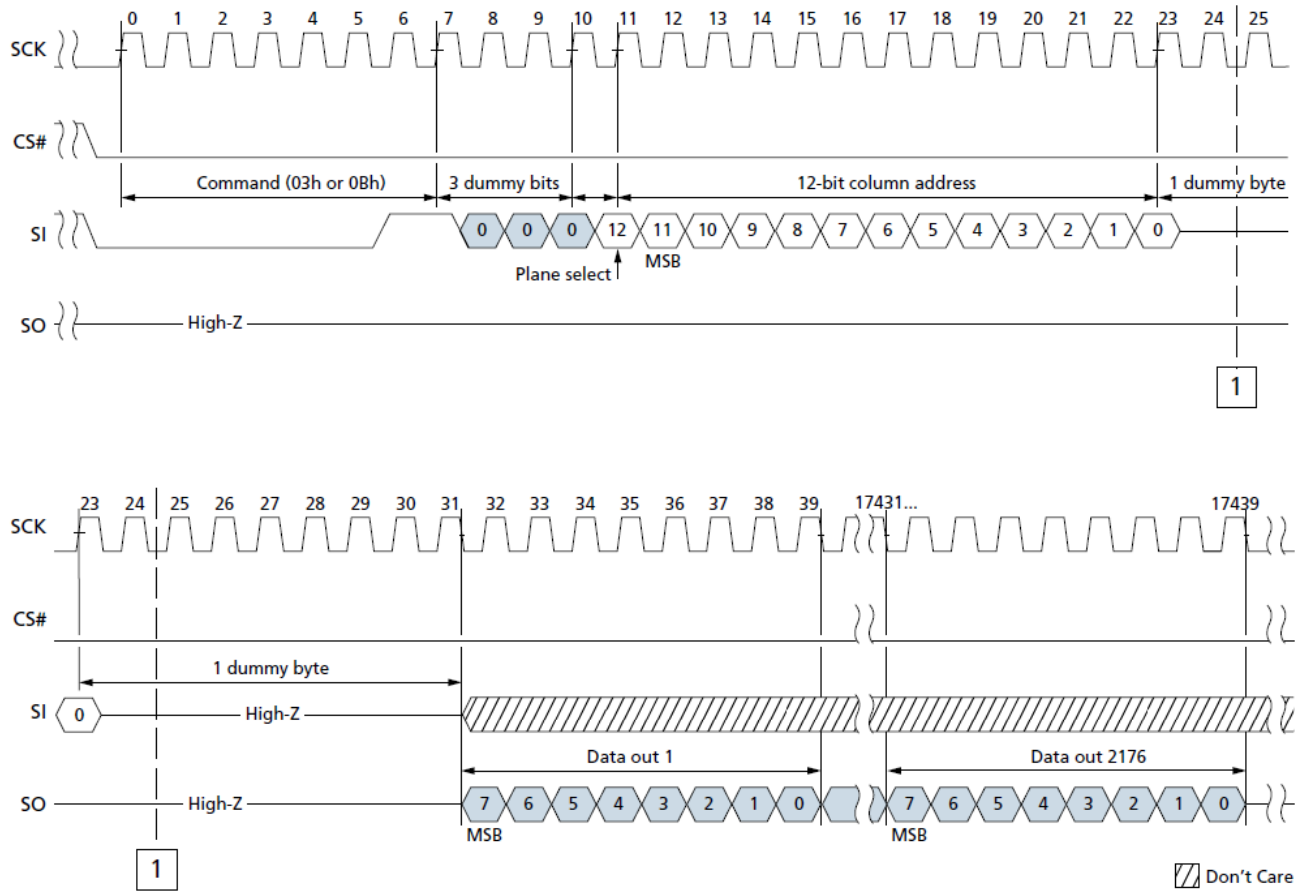


8.6 READ FROM CACHE X1 (03H OR 0BH)

The READ FROM CACHE x1 command (03h or 0Bh) enables sequentially reading one or more data bytes from the cache buffer. The command is initiated by driving CS# LOW, shifting in command opcode 03h/0Bh, followed by a 16 bit address.

Data is returned after 8-dummy clocks from the addressed cache buffer, MSB first, on SO at the falling edge of SCK. The address is automatically incremented to the next higher address after each byte of data shifted out, enabling a continuous stream of data. This command is completed by driving CS# HIGH.

Figure 8.6 READ from CACHE x1 (03h or 0Bh) Timing

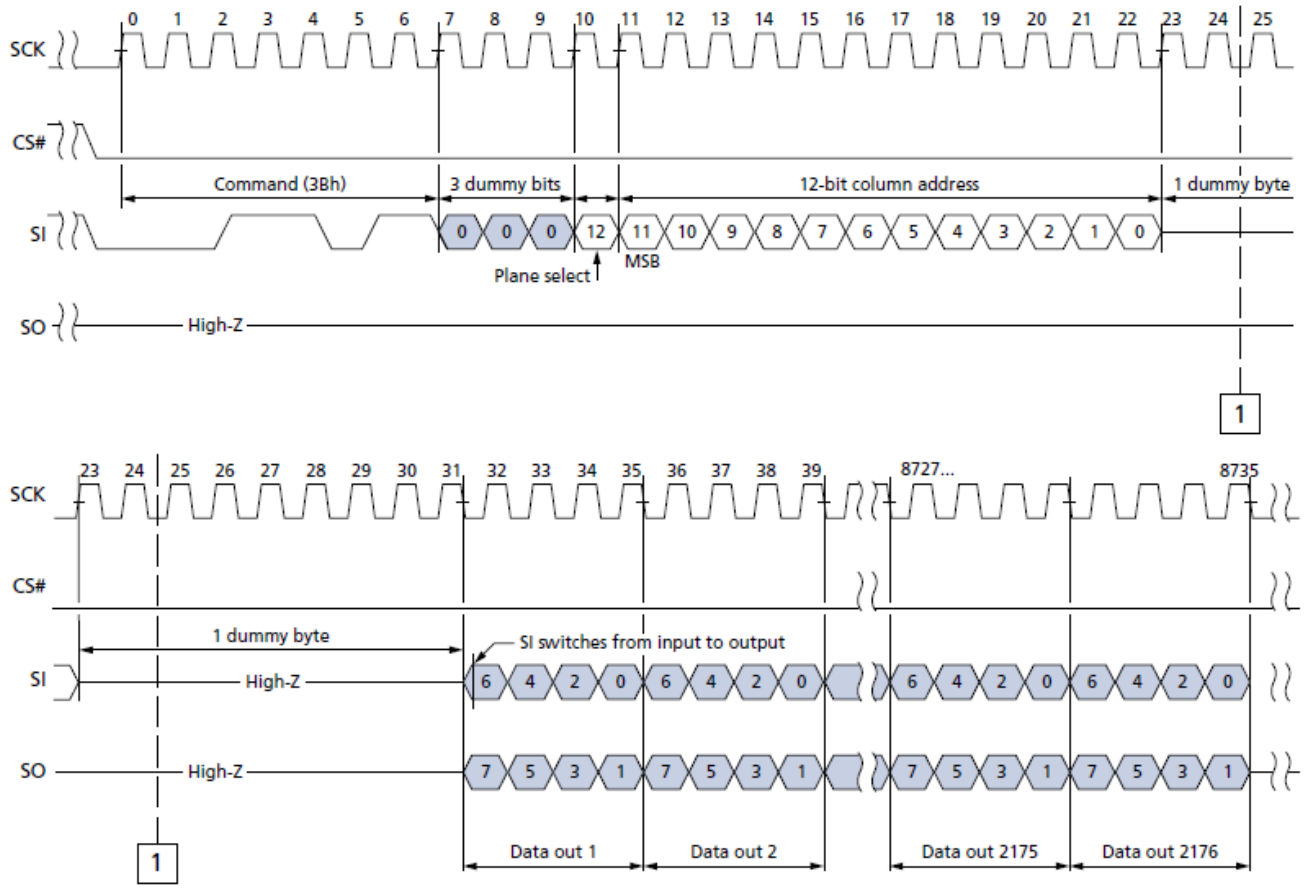


Note: Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.7 READ FROM CACHE X2 (3BH)

The READ FROM CACHE x2 (3Bh) command is similar to READ FROM CACHE x1 (03h or 0Bh), but output data is transferred through two pins, enabling data transfer at twice the rate: IO0 (SI) and IO1 (SO).

Figure 8.7 READ from CACHE x2 (3Bh) Timing

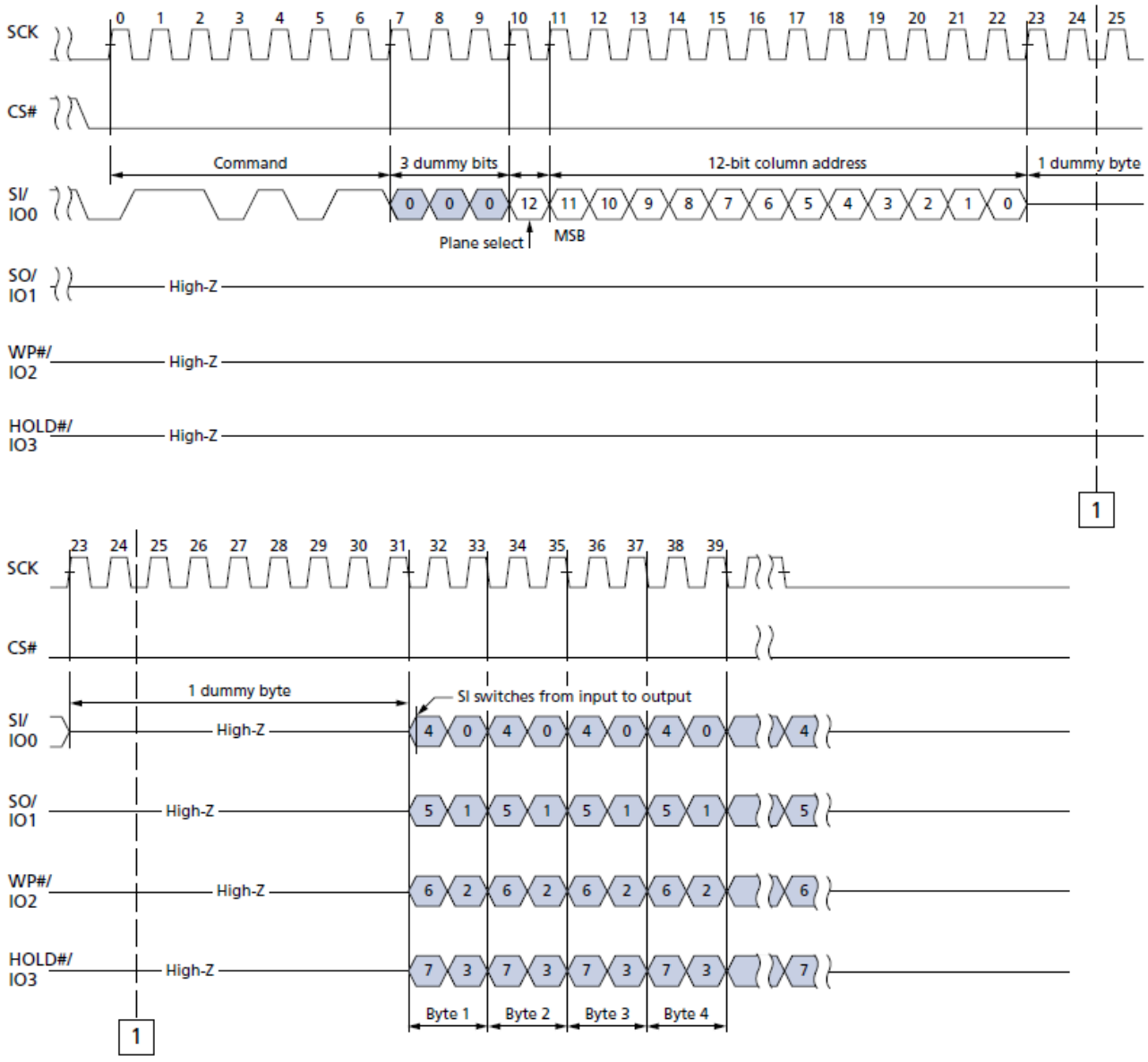


Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.8 READ FROM CACHE X4 (6BH)

The READ FROM CACHE x2 (3Bh) command is similar to READ FROM CACHE x1 (03h or 0Bh), but output data is transferred through four pins (IO0~IO3).

Figure 8.8 READ from CACHE x4 (6Bh) Timing

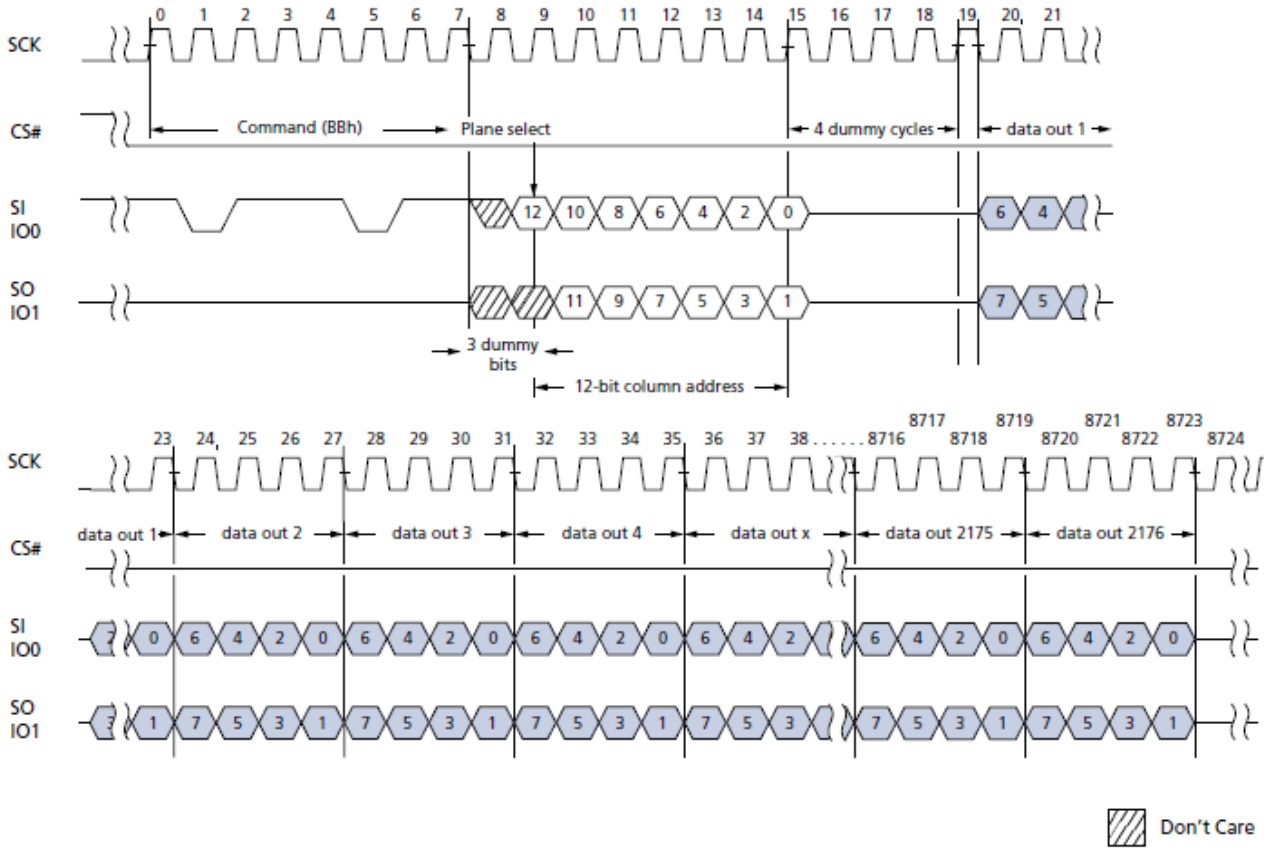


Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.9 READ FROM CACHE DUAL I/O (BBH)

The READ FROM CACHE Dual I/O (BBh) command enables improved random access while maintaining two I/O pins, IO0 and IO1. It is similar to the READ FROM CACHE x2 (3Bh) command, except that both address and data bits are input and output through two pins: IO0 and IO1. Also, there are 4-dummy cycles between address and data.

Figure 8.9 READ from CACHE DUAL I/O (BBh) Timing

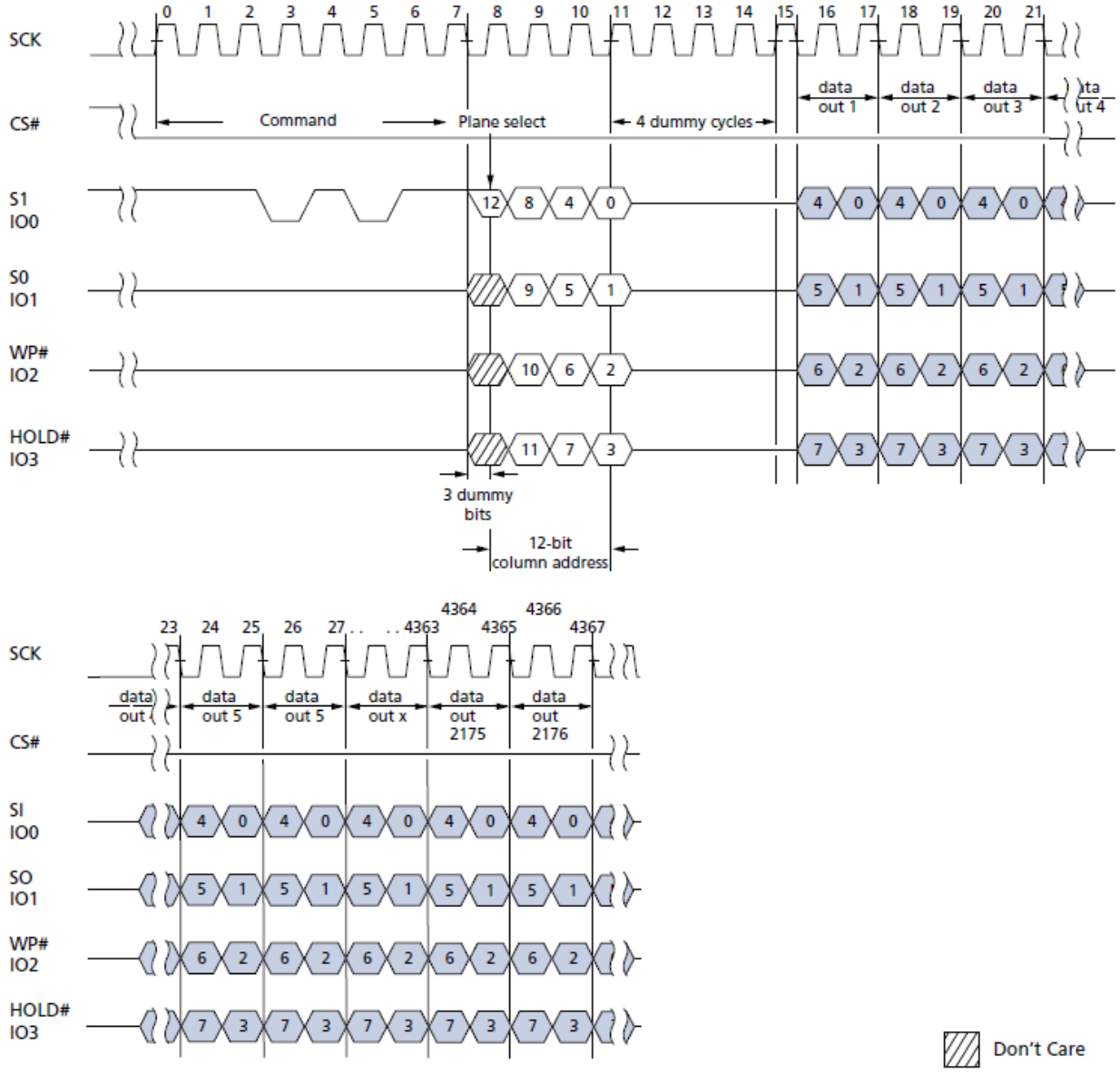


Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.10 READ FROM CACHE QUAD I/O (EBH)

The READ FROM CACHE Quad I/O (EBh) command is similar to READ FROM CACHE Dual I/O (BBh) command except that address and data bits are input and output through four pins: IO0, IO1, IO2, and IO3. Also, there are 4-dummy cycles between address and data.

Figure 8.10 READ from CACHE Quad I/O (EBh) Timing



Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.11 READ PAGE CACHE RANDOM (30H)

The READ PAGE CACHE RANDOM (30h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die when it is ready (OIP=0, CRBSY=0). This command is used to improve the read throughput as follows:

1. 13h – PAGE READ to CACHE
2. 0Fh – GET FEATURE command to read status until OIP status bit is changed from 1 to 0
3. **30h – READ PAGE CACHE RANDOM command to transfer data from data register to cache register and kick off the next page transfer from array to data register**
4. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0
5. 03h, 0Bh, 3Bh, 6Bh, BBh, or EBh – READ FROM CACHE TO OUTPUT command
6. 0Fh – GET FEATURE command to read the status until CRBSY = 0
7. Repeat step 3 to step 6 to read out all expected pages until last page
8. **3Fh – READ PAGE CACHE LAST command to end the read page cache sequence and copy a last page from the data register to the cache register**
9. 0Fh – GET FEATURE command to read the status until OIP status bit is changed from 1 to 0
10. 03h, 0Bh, 3Bh, 6Bh, BBh, or EBh – READ FROM CACHE TO OUTPUT command to read out last page from cache register to output

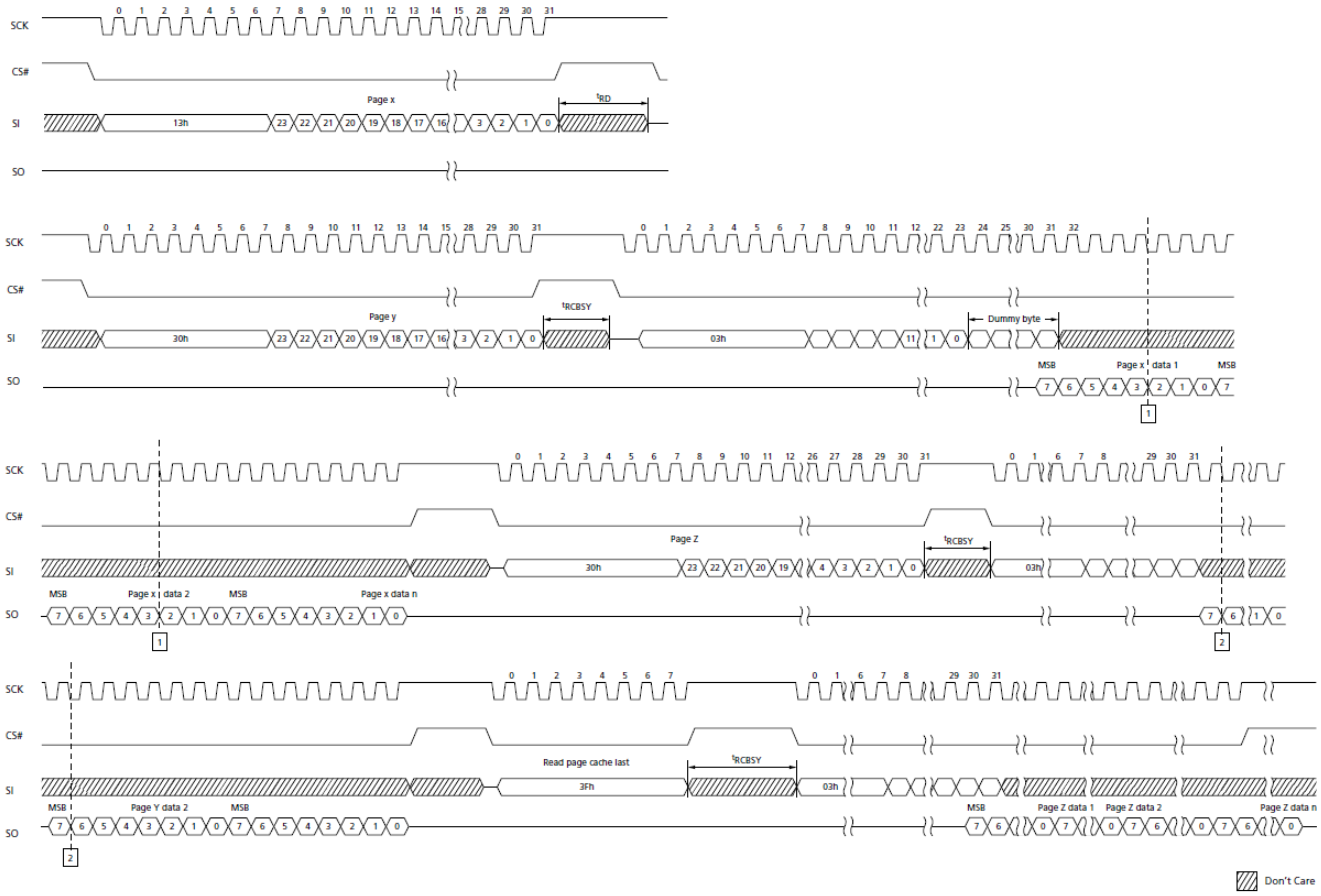
The READ PAGE CACHE RANDOM command requires a 24 bit address (dummy bits + valid block/page address).

After the block/page addresses are registered, the device starts to transfer data from data register to cache register for tRCBSY. After tRCBSY, OIP bit (through GET FEATURE command to check this status bit) goes to 0 from 1, indicating that the cache register is available and that the specified page in the READ PAGE CACHE RANDOM command is copying from the Flash array to the data register.

At this point, data can be output from the cache register beginning at the column address specified by READ FROM CACHE commands.
The status register CRBSY bit value remains at 1, indicating that the specified page in READ PAGE CACHE RANDOM command is copying from the cell array to the data register; CRBSY returns to 0 to indicating the copying from array is completed. During tRCBSY, the error check and correction is also performed.

Note: When On-Chip ECC is ON, ECC is executed after data is transferred from the data register to the cache register; therefore, tCRBSY includes the ECC time, which must be factored in when checking the OIP status.

Figure 8.11 READ PAGE CACHE RANDOM Sequence



8.12 READ PAGE CACHE LAST (3FH)

The READ PAGE CACHE LAST (3Fh) command ends the READ PAGE CACHE RANDOM sequence and copies a page from the data register to the cache register.

This command is accepted by the die when it is ready (OIP=0, CRBSY=0).

After the command is issued, the status register bit OIP goes HIGH and the device is busy (CRBSY=0, OIP=1) for tCRBSY. Address is not applied in this command sequence. When data is completely copied to cache register, OIP goes LOW and READ FROM CACHE commands could be issued to output data.

8.13 PAGE PROGRAM OPERATIONS

A PAGE PROGRAM operation sequence enables the host to input 1 byte to 2176 bytes of data within a page to a cache register, and moves the data from the cache register to the specified block and page addresses in the array.

- **If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register**

The page program sequence is as follows:

- 06h (Write Enable command)
- 02h (Program Load command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURES command to read the status)

8.14 PROGRAM LOAD X1 (02H)

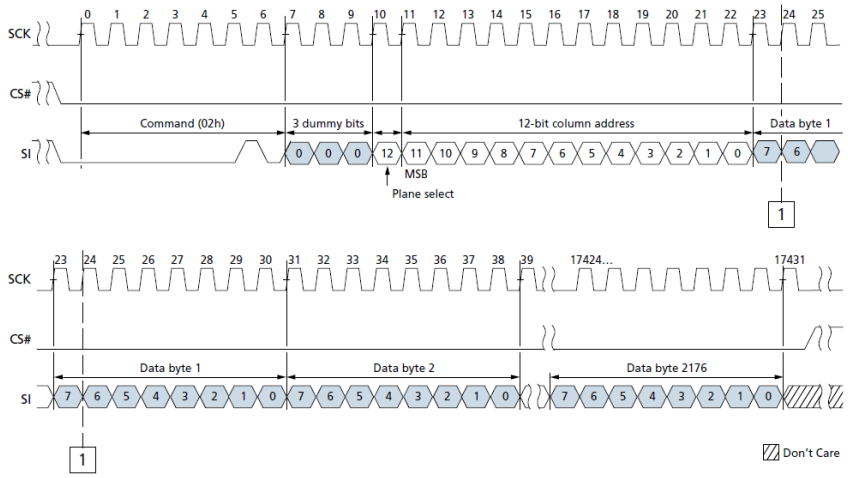
Prior to performing PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be issued in order to set WEL bit. WRITE ENABLE is followed by a PROGRAM LOAD (02h) command.

The PROGRAM LOAD command consists of an 8-bit opcode, followed by 16 bit address, and then the data bytes to be programmed.

The data bytes are loaded into a cache register that is 2176 bytes long. **Only four partial page programs are allowed on a single page.**

The command sequence ends when CS# goes from LOW to HIGH.

Figure 8.12 PROGRAM LOAD x1 (02h) Timing



Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

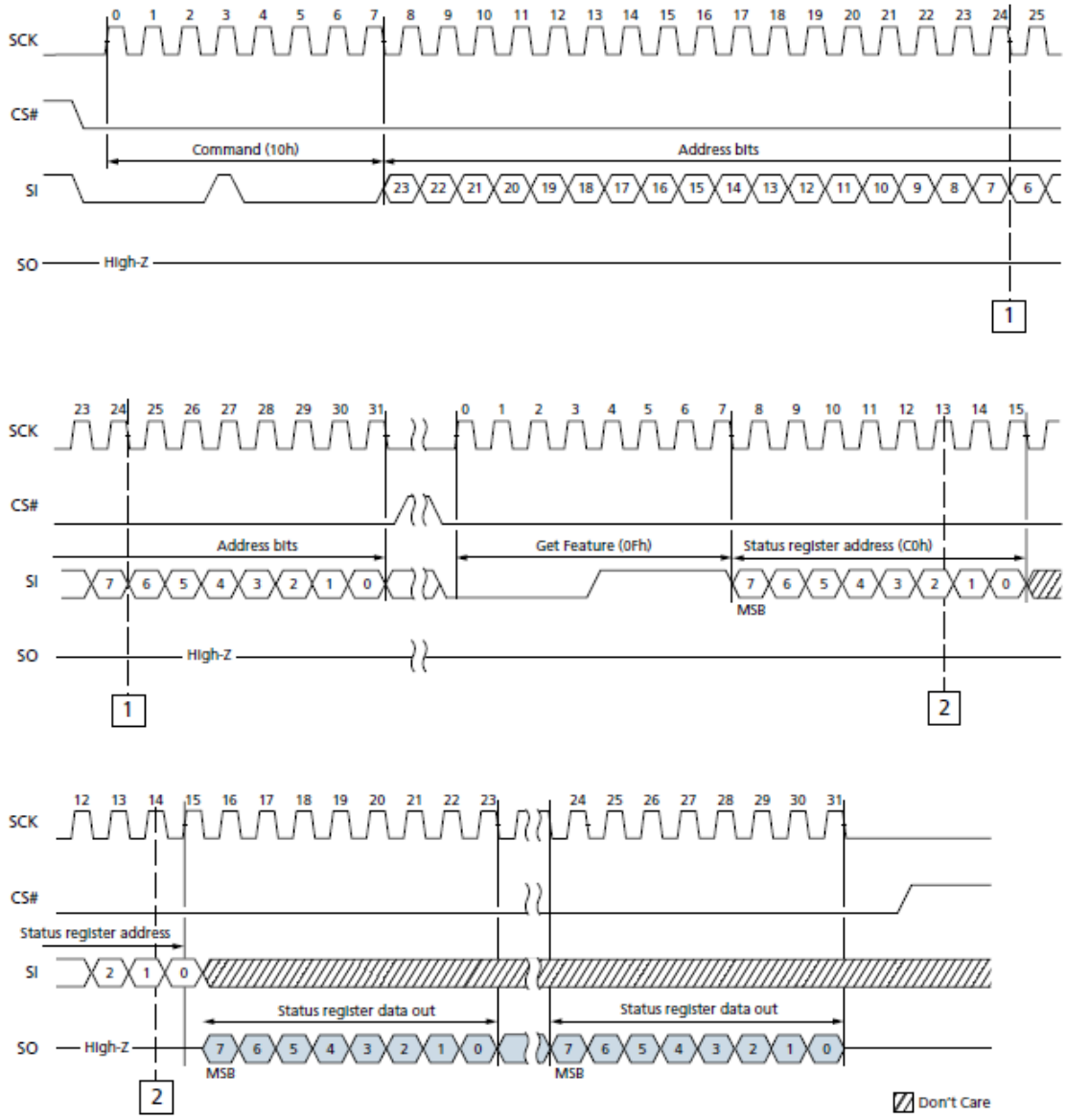
8.15 PROGRAM EXECUTE (10H)

The PROGRAM EXECUTE command consists of an 8-bit op code, followed by a 24-bit address (dummy bits + valid page/block address - 16 addresses for 1Gb, 17 addresses for 2/4/8Gb).

After the page/block address is registered, **the device starts the transfer from the cache register to the main array** and is busy for tPROG time.

During this busy time, the status register can be polled to monitor the status of the operation. When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure 8.13 PROGRAM EXECUTE TIMING



8.16 RANDOM DATA PROGRAM X1 (84H)

The RANDOM DATA PROGRAM operation programs or replaces data in a page with existing data. The RANDOM DATA PROGRAM sequence is as follows:

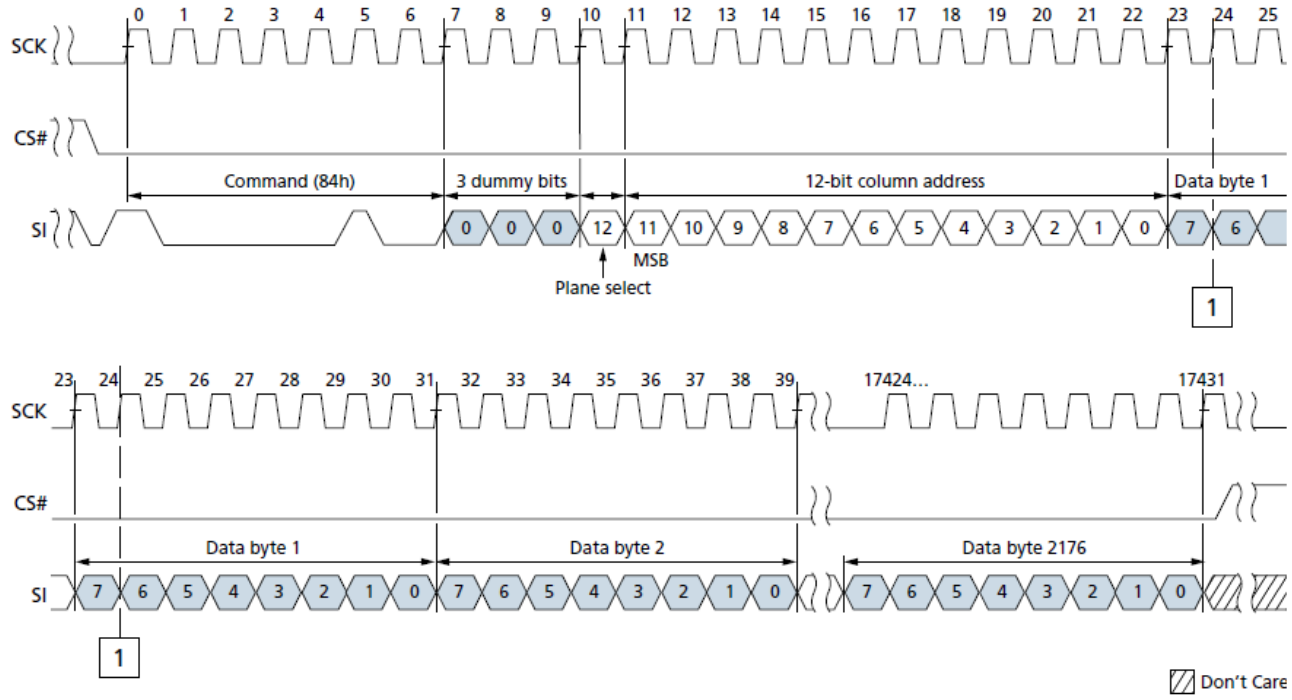
- 06h (WRITE ENABLE command)
- **84h (PROGRAM LOAD RANDOM DATA command)**
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURES command to read the status)

The PROGRAM LOAD RANDOM DATA x1 (84h) operation is similar to PROGRAM LOAD x1 (02h).

The difference is that PROGRAM LOAD x1 command will reset cache buffer to an all FFh value, while RANDOM LOAD x1 command will only update the data bytes that are specified by the command input sequence, and the rest of data in the cache buffer will remain unchanged.

If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA x1 (84h) command must be issued with a new column address. After data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Figure 8.14 PROGRAM LOAD RANDOM DATA (84h) Timing

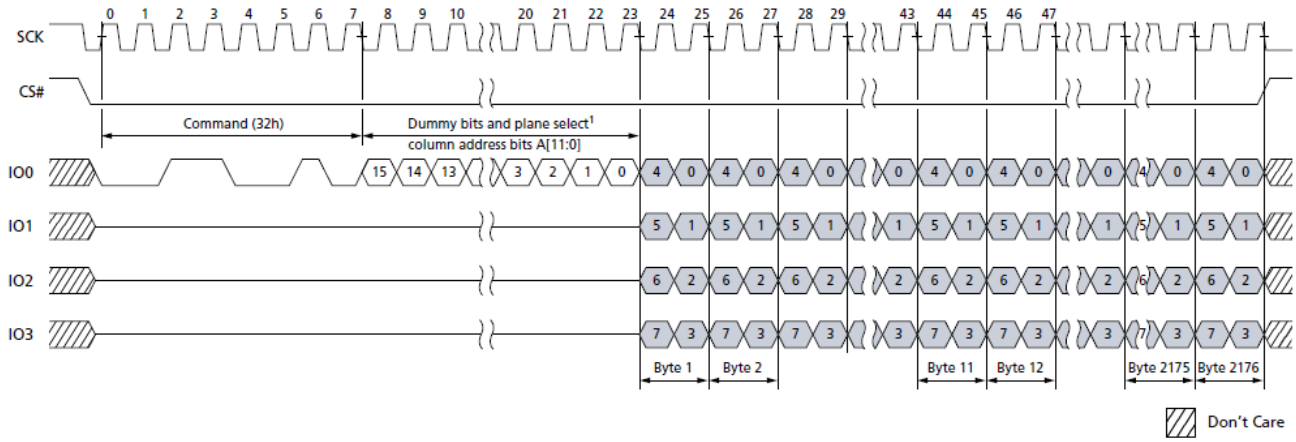


Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.17 PROGRAM LOAD X4 (32H) AND PROGRAM LOAD RANDOM DATA X4 (34H)

The PROGRAM LAOD x4 (32h) and RANDOM DATA x4 (34h) is similar to PROGRAM LOAD x1 (02h) command and RANDOM DATA x1 (84h), **but with the capability to input the data across for data lines**.

Figure 8.15 PROGRAM LOAD x4 (32h) Timing



Note: 1. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

8.18 INTERNAL DATA MOVE

The INTERNAL DATA MOVE command programs or replaces data in a page with existing data. The internal data move command sequence is as follows:

- **13h (PAGE READ command to cache)**
- 06h (WRITE ENABLE command)
- 84h (PROGRAM LOAD RANDOM DATA command)
- 10h (PROGRAM EXECUTE command)
- 0Fh (GET FEATURES command to read status)

Note: If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h) command must be issued with the new column address.

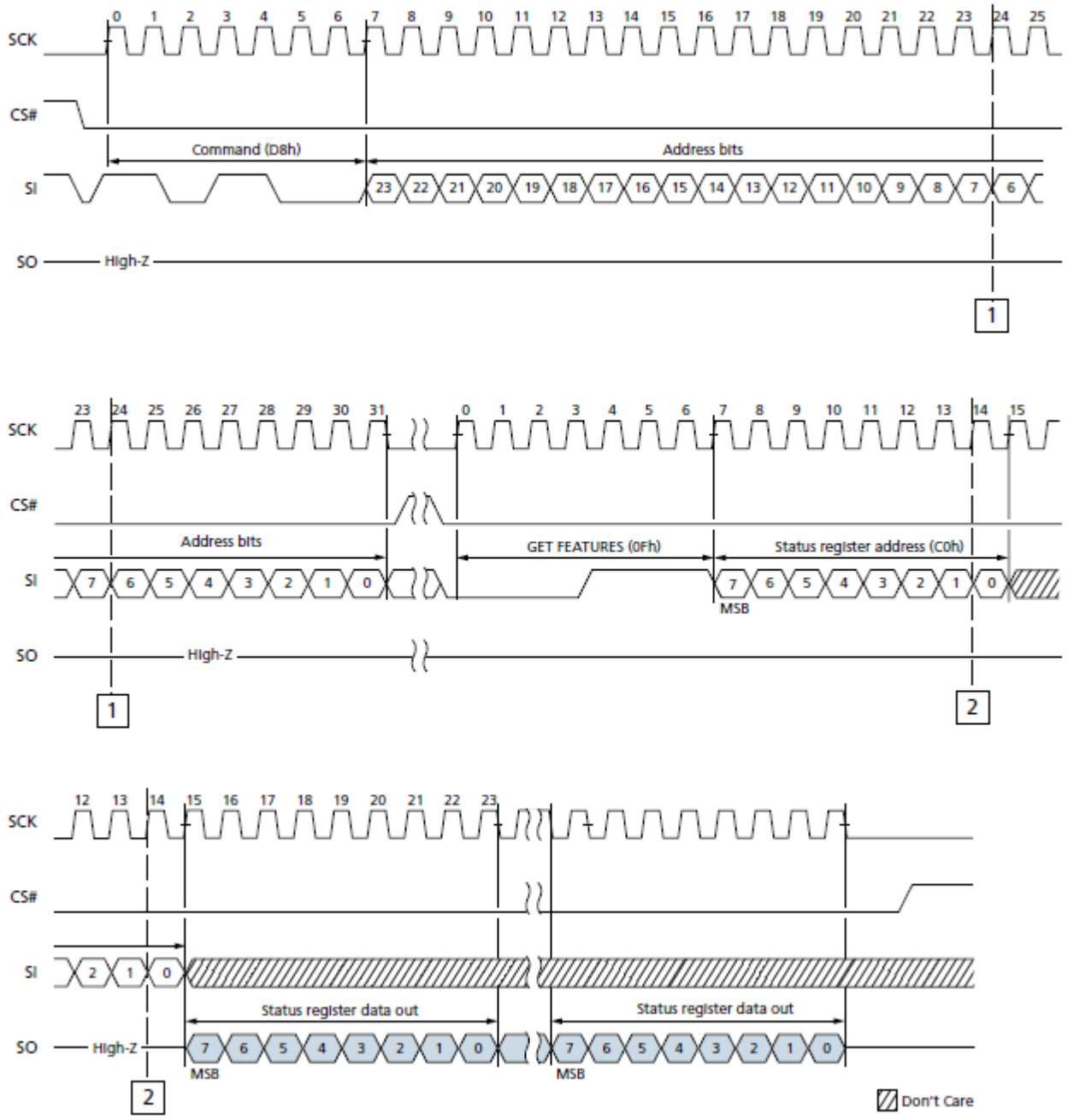
8.19 BLOCK ERASE OPERATIONS

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). The BLOCK ERASE command (D8h) operations on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENABLE command)
- **D8h (BLOCK ERASE command)**
- 0Fh (GET FEATURES command to read the status register).

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be excuted in order to set the WEL bit. If the WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires **24-bit address** consisting of dummy bits and valid block/page address. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation.

Figure 8.16 BLOCK ERASE (D8h) Timing



8.20 ECC PROTECTION

The device offers an 8-bit data corruption protection by offering On Chip ECC to obtain the data integrity. The On Chip ECC can be enabled or disabled by ECC_EN bit in the configuration register. **ECC is enabled after power-up by default**. Reset will not change the existing configuration. To enable/disable ECC after power on, perform the following command sequence:

- Issue SET FEATURES command (1Fh)
- **Issue configuration register address (B0h)**
- Set bit 4 to 1 to enable ECC; Clear bit 4 to 0 to disable ECC.

During a program operation, the device calculates an expected ECC code on the ECC protected bytes in the cache register, before the page is written to the Flash array. The ECC code is stored in the spare area of the page.

During a read operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the expected ECC code value read from the array. If a 1to 8 bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status register bit indicates whether or not the error correction is successful. .

The Unique ID and parameter page are not ECC protected areas.

Multiple copies are provided for parameter page to obtain the data integrity. XOR method is provided for Unique ID to verify data.

With On Chip ECC, users must accommodate the following.

- Spare area definitions
- **WRITEs are supported for main and spare areas (User meta table I and II). WRITEs to the ECC area are prohibited.**

When using partial-page programming, the following conditions must be met:

- Main user area and user meta data area I – **Single partial-page programming operations must** be used.
- **Within a page, a maximum of four partial-page programming operations can be performed.**

Table 8.4 ECC Status Register Bit Descriptions

ECCS[2:0]	ECC Status
000	No bit error
001	1-3 bit errors detected and corrected.
010	**Bit errors greater than 8 bites detected and uncorrectable**
011	4-6 bit errors detected and corrected.
101	7-8 bit errors detected and corrected. Indicates data refreshment must be taken to guarantee data retention
Others	Reserved

Table 8.5 Spare Area Mapping

Max Byte Address	Min Byte Address	ECC Protected	Area	Area Size	Description
1FFh	000h	Yes	Main 0	512KB	User data
3FFh	200h	Yes	Main 1	512KB	User data
5FFh	400h	Yes	Main 2	512KB	User data
7FFh	600h	Yes	Main 3	512KB	User data
803h	800h	No	Spare 0	4B	Reserved (1)
807h	804h	No	Spare 1	4B	User Metadata II
80Bh	808h	No	Spare 2	4B	
80Fh	80Ch	No	Spare 3	4B	
813h	810h	No	Spare 0	4B	User Metadata II
817h	814h	No	Spare 1	4B	
81Bh	818h	No	Spare 2	4B	
81Fh	81Ch	No	Spare 3	4B	
827h	820h	Yes	Spare 0	8B	User Metadata I
82Fh	828h	Yes	Spare 1	8B	
837h	830h	Yes	Spare 2	8B	
83Fh	838h	Yes	Spare 3	8B	
84Fh	840h	Yes	Spare 0	16B	ECC for main/spare 0
85Fh	850h	Yes	Spare 1	16B	ECC for main/spare 1
86Fh	860h	Yes	Spare 2	16B	ECC for main/spare 2
87Fh	870h	Yes	Spare 3	16B	ECC for main/spare 3

Note:

1. **Reserved for Bad Block Information**

8.21 ERROR MANAGEMENT

The NAND Flash is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the device could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per device will not fall below NVB during the endurance life of the product.

Although the device could contain bad blocks, they can be used quite reliably in systems that provide bad block management and error correction algorithms.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the blocks.

The NAND device is shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad block mark into every location in the first page of each invalid block.

The first byte in the spare area of the first page and second page of each block are guaranteed to contain the bad block mark. This method is compliant with ONFI Factory Defect Mapping requirements.

A host controller has to check the spare area location for non-FF data on the first page or second page of each block prior to performing any PROGRAM or ERASE operations. A bad block table can then be created, enabling system software to map around these areas.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required.

- Always check status after a PROGRAM or ERASE operation.
- Under typical conditions, use the minimum required ECC.
- Use Bad block management and wear-leveling algorithm.

Table 8.6 Error Management Details

Description		**Requirement**
Minimum number of valid blocks (NVB) per die (LUN)	1Gb	1004
	2Gb(1)	2008
Total available blocks per die (LUN)	1Gb	1024
	2Gb(1)	2048
First spare area location in the first page of each block		Byte 2048
Value programmed for **bad block** at the first byte of spare area		00h
Minimum ECC with On Chip ECC enabled		8-bit ECC per 512 bytes (user data) + 8 bytes (spare) + 16 bytes (ECC data)

Note:

1. 4Gb is 2 die of 2Mb, 8Gb is 4 die of 2Gb.

8.22 SPI NOR COMPATIBLE READ OPERATION

Address allocation in SPI NAND read from cache x1 protocol is 16 byte, so it is different from address allocation of **24 bit in traditional SPI NOR read protocol**.

The device offers an alternative solution to implement 03h/0Bh commands, as are done with SPI NOR, to be drop-in compatible to SPI NOR read protocol.

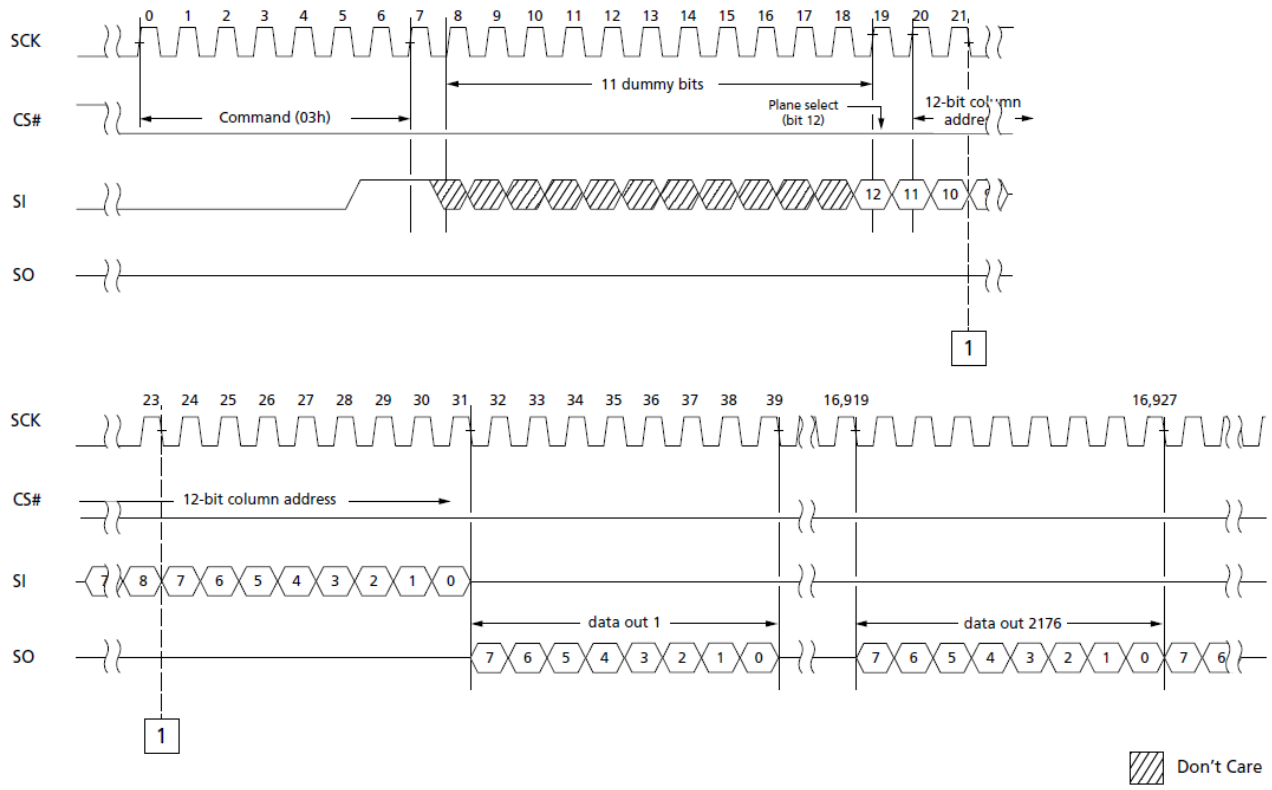
Refer to the Electrical Specifications for detail timing requirement.

Command sequence to enter into SPI NOR read mode:

- SET FEATURE command (1Fh) with feature address B0h and CFG bits [2:0] = **101b** (enter into SPI NOR read protocol enable mode)
- WRITE ENABLE command (06h)
- PROGRAM EXECUTE command (10h) with block/page address all 0
- GET FEATURE command (0Fh) with status register address C0h to check until device is ready (OIP bit clear) and verify that P_FAIL bit is not set.
- SET FEATURE command (1Fh) with feature address B0h and CFG bits [2:0] = **000b** (return to normal operation mode)
- GET FEATURE command (0Fh) with address B0h and CFG bits [2:0] = **101b** to verify all 0; all 1 indicates SPI NOR read mode not enabled.

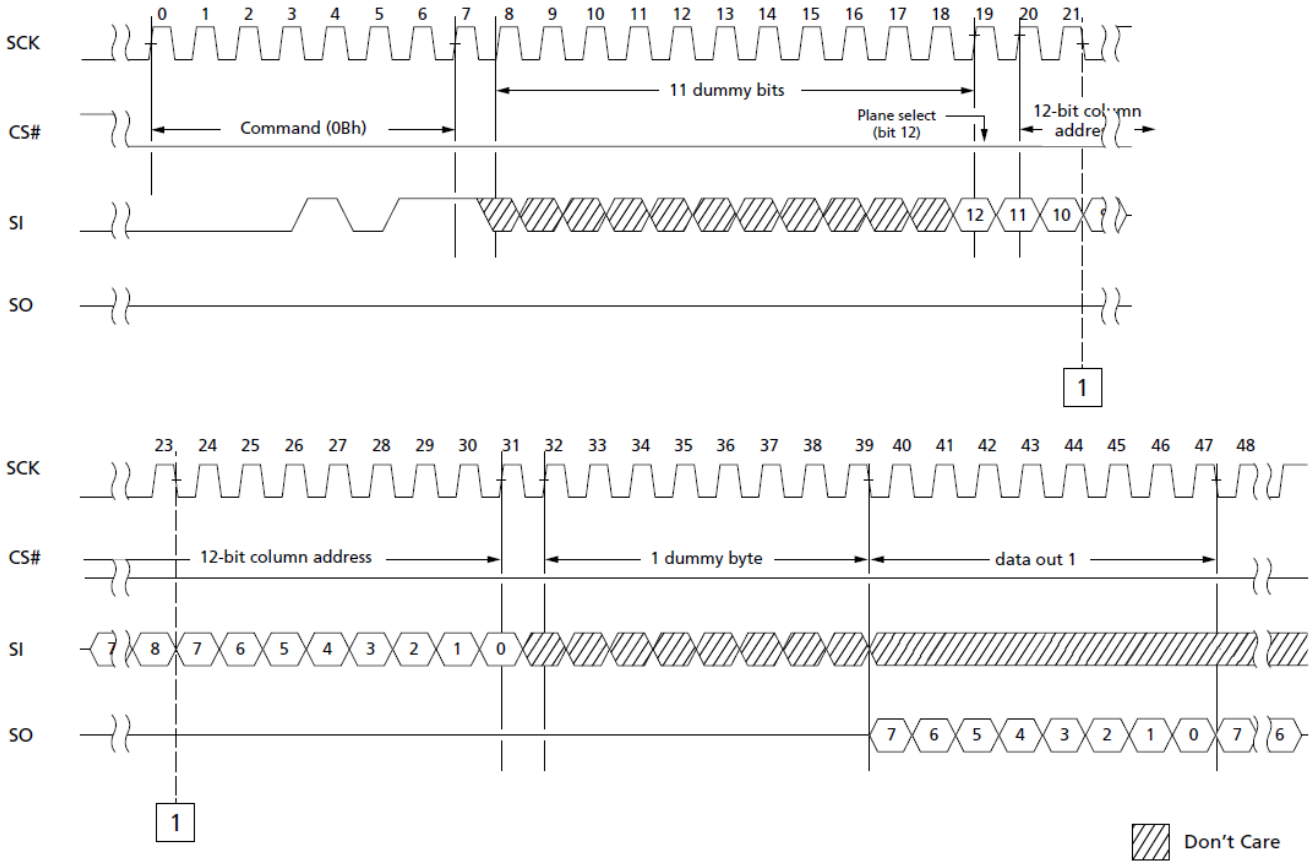
Note: It is an OTP configuration setting and it cannot recover to SPI NAND default mode, even after power cycle. The rest of the SPI NAND commands except for 03h/0Bh commands still work in this configuration.

Figure 8.17 Read from Cache (03h) in SPI NOR mode



Note: 1. SPI NOR compatible mode. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

Figure 8.18 Fast Read from Cache (0Bh) in SPI NOR mode



Note: 1. SPI NOR compatible mode. Plane select bit is not available in 1Gb device and can be used as a dummy bit.

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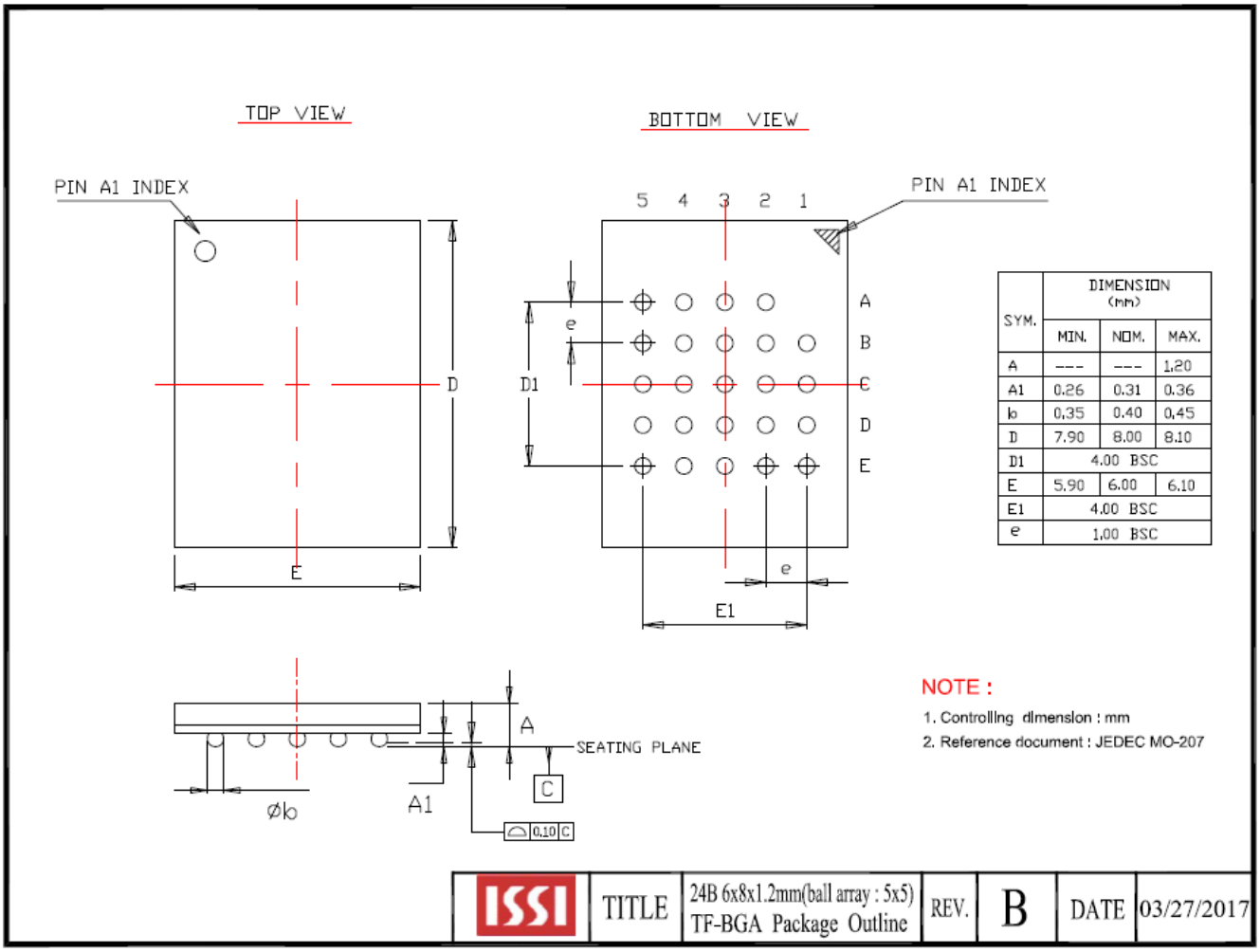
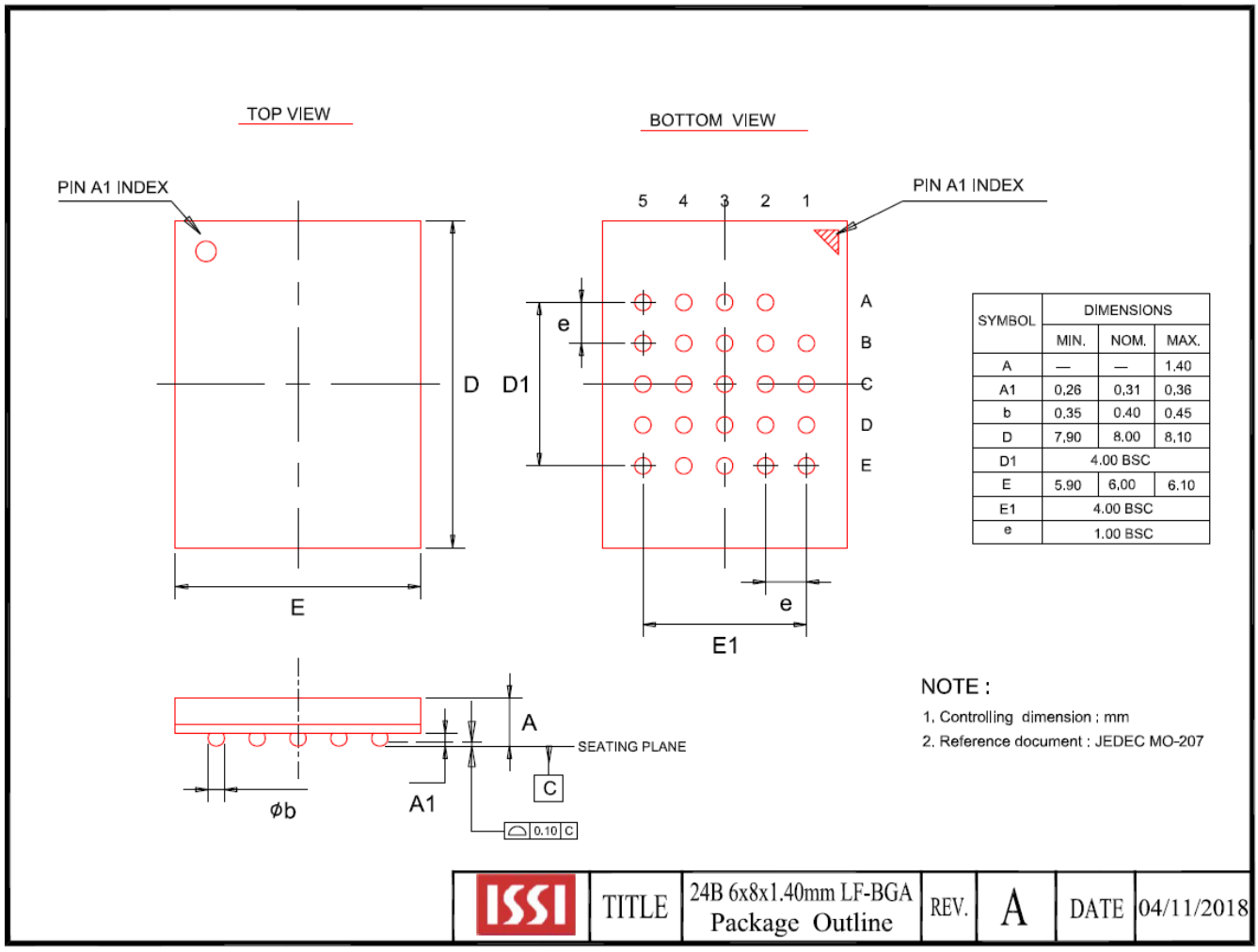
9. PACKAGE INFORMATION

9.1 24-BALL THIN PROFILE FINE PITCH BGA 6X8X1.2MM 5X5 BALL ARRAY (H)



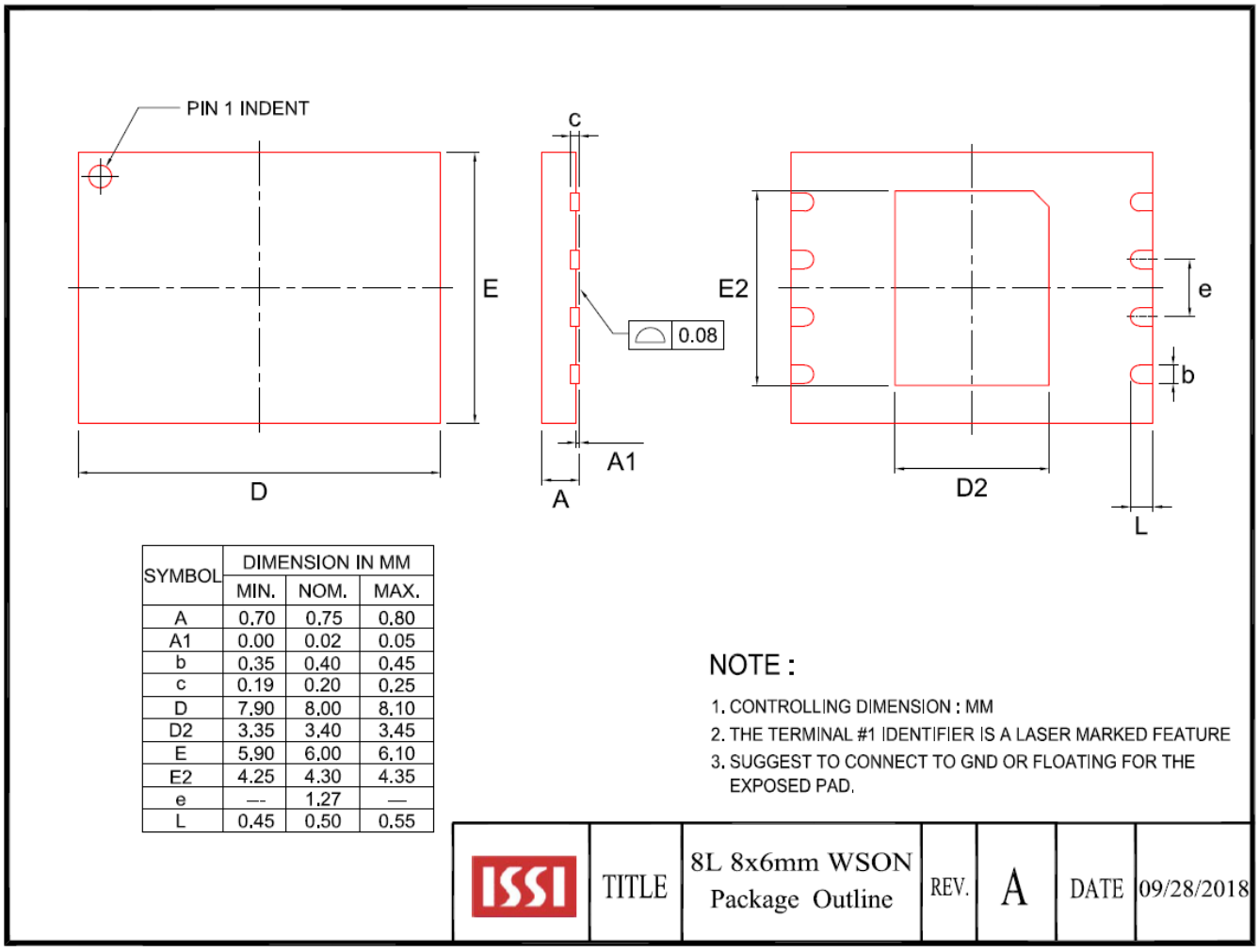
SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

9.2 24-BALL THIN PROFILE FINE PITCH BGA 6X8X1.4MM 5X5 BALL ARRAY (I)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.40
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

9.3 8- CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 8X6MM (J)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
c	0.19	0.20	0.25
D	7.90	8.00	8.10
D2	3.35	3.40	3.45
E	5.90	6.00	6.10
E2	4.25	4.30	4.35
e	---	1.27	---
L	0.45	0.50	0.55

NOTE :

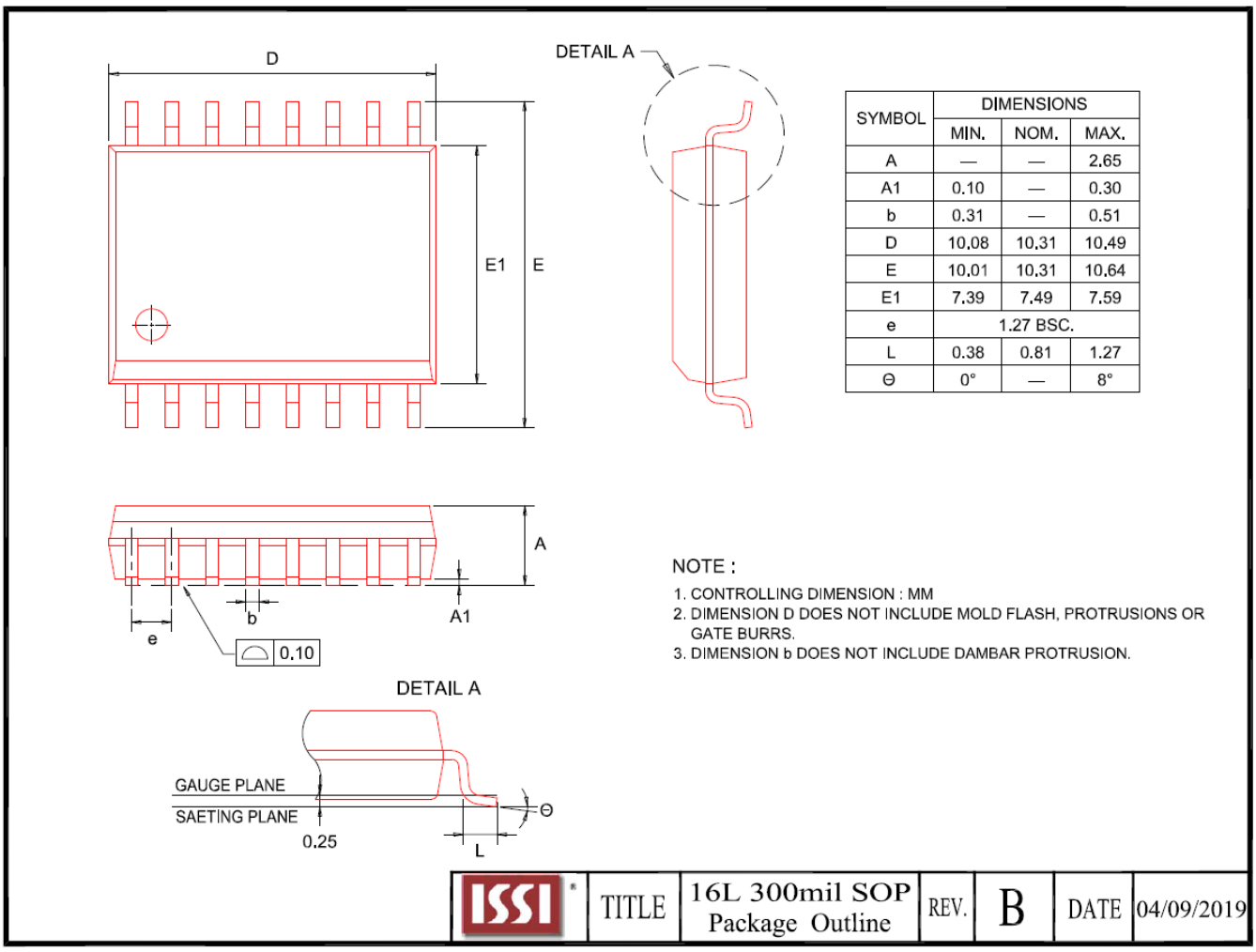
1. CONTROLLING DIMENSION : MM
2. THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE
3. SUGGEST TO CONNECT TO GND OR FLOATING FOR THE EXPOSED PAD.

	TITLE	8L 8x6mm WSON Package Outline	REV.	A	DATE	09/28/2018

Notes:

1. Please **click here** to refer to Application Note (AN25D011, Thin USON/WSON/XSON package handling precautions) for assembly guidelines.
2. **Pad Open size is 3.4mm x 4.3mm**

9.4 16- LEAD PLASTIC SMALL OUTLINE PACKAGE (300 MILS BODY WIDTH (M)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.65
A1	0.10	—	0.30
b	0.31	—	0.51
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC.		
L	0.38	0.81	1.27
Θ	0°	—	8°

NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

TITLE	16L 300mil SOP Package Outline	REV.	B	DATE	04/09/2019

10. ORDERING INFORMATION – Valid Part Numbers

IS 37 SM W 04G 8 A - J H L I

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A1 = Automotive Grade (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = **RoHS compliant**

PACKAGE Type
H = 24-ball TFBGA 6x8x1.2 mm
I = 24-ball LFBGA 6x8x1.4 mm (8Gb only, Call Factory)
J = 8-contact WSON (8x6mm), Pad Open = 3.4mmx4.3mm
M = 16-pin SOIC 300mil

Option
J=Normal

Die Revision
A = Gen. A

ECC Requirement
8 = 8-bit ECC

Density
01G = 1Gb
02G = 2Gb
04G = 4Gb
08G = 8Gb (LFBGA only, Call Factory)

VDD
W = 1.8V
L = 3.0V

Technology
SM = SPI-NAND (SLC)

Product Family
37 = SPI-NAND
38 = Automotive SPI-NAND

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.

Note:
1. Call Factory for other package options available.

VDD	Density	Temp. Grade	Order Part Number	Package
3.0V	1Gb	Industrial	IS37SML01G8A-JJLI	8-contact WSON 8x6mm
			IS37SML01G8A-JMLI	16-pin SOIC 300mil
			IS37SML01G8A-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A1)	IS38SML01G8A-JJLA1	8-contact WSON 8x6mm
			IS38SML01G8A-JMLA1	16-pin SOIC 300mil
			IS38SML01G8A-JHLA1	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SML01G8A-JJLA2	8-contact WSON 8x6mm
			IS38SML01G8A-JMLA2	16-pin SOIC 300mil
			IS38SML01G8A-JHLA2	24-ball TFBGA 6x8x1.2 mm
	2Gb	Industrial	IS37SML02G8A-JJLI	8-contact WSON 8x6mm
			IS37SML02G8A-JMLI	16-pin SOIC 300mil
			IS37SML02G8A-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A1)	IS38SML02G8A-JJLA1	8-contact WSON 8x6mm
			IS38SML02G8A-JMLA1	16-pin SOIC 300mil
			IS38SML02G8A-JHLA1	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SML02G8A-JJLA2	8-contact WSON 8x6mm
			IS38SML02G8A-JMLA2	16-pin SOIC 300mil
			IS38SML02G8A-JHLA2	24-ball TFBGA 6x8x1.2 mm
	4Gb	Industrial	IS37SML04G8A-JJLI	8-contact WSON 8x6mm
			IS37SML04G8A-JMLI	16-pin SOIC 300mil
			IS37SML04G8A-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A1)	IS38SML04G8A-JJLA1	8-contact WSON 8x6mm
			IS38SML04G8A-JMLA1	16-pin SOIC 300mil
			IS38SML04G8A-JHLA1	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SML04G8A-JJLA2	8-contact WSON 8x6mm
			IS38SML04G8A-JMLA2	16-pin SOIC 300mil
			IS38SML04G8A-JHLA2	24-ball TFBGA 6x8x1.2 mm

Note:
1. A1, A2 meet AEC-Q100 requirements with PPAP.
Temp Grades: A1= -40 to 85°C, A2= -40 to 105°C

VDD	Density	Temp. Grade	Order Part Number	Package
1.8V	1Gb	Industrial	IS37SMW01G8A-JJLI	8-contact WSON 8x6mm
			IS37SMW01G8A-JMLI	16-pin SOIC 300mil
			IS37SMW01G8A-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A1)	IS38SMW01G8A-JJLA1	8-contact WSON 8x6mm
			IS38SMW01G8A-JMLA1	16-pin SOIC 300mil
			IS38SMW01G8A-JHLA1	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SMW01G8A-JJLA2	8-contact WSON 8x6mm
			IS38SMW01G8A-JMLA2	16-pin SOIC 300mil
			IS38SMW01G8A-JHLA2	24-ball TFBGA 6x8x1.2 mm
	2Gb	Industrial	IS37SMW02G8A-JJLI	8-contact WSON 8x6mm
			IS37SMW02G8A-JMLI	16-pin SOIC 300mil
			IS37SMW02G8A-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A1)	IS38SMW02G8A-JJLA1	8-contact WSON 8x6mm
			IS38SMW02G8A-JMLA1	16-pin SOIC 300mil
			IS38SMW02G8A-JHLA1	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SMW02G8A-JJLA2	8-contact WSON 8x6mm
			IS38SMW02G8A-JMLA2	16-pin SOIC 300mil
			IS38SMW02G8A-JHLA2	24-ball TFBGA 6x8x1.2 mm
	4Gb	Industrial	IS37SMW04G8A-JJLI	8-contact WSON 8x6mm
			IS37SMW04G8A-JMLI	16-pin SOIC 300mil
			IS37SMW04G8A-JHLI	24-ball TFBGA 6x8x1.2 mm
		Automotive (A1)	IS38SMW04G8A-JJLA1	8-contact WSON 8x6mm
			IS38SMW04G8A-JMLA1	16-pin SOIC 300mil
			IS38SMW04G8A-JHLA1	24-ball TFBGA 6x8x1.2 mm
		Automotive (A2)	IS38SMW04G8A-JJLA2	8-contact WSON 8x6mm
			IS38SMW04G8A-JMLA2	16-pin SOIC 300mil
			IS38SMW04G8A-JHLA2	24-ball TFBGA 6x8x1.2 mm

Note:
1. A1, A2 meet AEC-Q100 requirements with PPAP.
Temp Grades: A1= -40 to 85°C, A2= -40 to 105°C