FEATURES

- High-speed access times:
  - 10 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
  - 60 µW (typical) CMOS standby
  - 65 mW (typical) operating
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs
- Lead-free available

DESCRIPTION

The ISSI IS61LV256AL is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns maximum.

When \( \overline{CE} \) is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 150 µW (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable (\( \overline{CE} \)). The active LOW Write Enable (\( WE \)) controls both writing and reading of the memory.

The IS61LV256AL is available in the JEDEC standard 28-pin, 300-mil SOJ and the 450-mil TSOP (Type I) packages.
PIN CONFIGURATION
28-Pin SOJ

22
23
24
25
26
27
28
1
2
3
4
5
6
7
21
20
19
18
17
16
15
14
13
12
11
10
9
8
OE
A11
A9
A8
A13
WE
VDD
A14
A12
A7
A6
A5
A4
A3
A2
A1
A0
I/O0
I/O1
I/O2
I/GND

PIN DESCRIPTIONS
A0-A14 Address Inputs
CE Chip Enable Input
OE Output Enable Input
WE Write Enable Input
I/O0-I/O7 Input/Output
VDD Power
GND Ground

PIN CONFIGURATION
28-Pin TSOP (Type I)

OE
22
A11
A9
A8
A13
WE
VDD
A14
A12
A7
A6
A5
A4
A3
I/O0
I/O1
I/O2
I/GND

TRUTH TABLE

Mode | WE | CE | OE | I/O Operation | VDD Current |
--- | --- | --- | --- | --- | --- |
Not Selected (Power-down) | X | H | X | High-Z | Isb1, Isb2 |
Output Disabled | H | L | H | High-Z | ICC |
Read | H | L | L | DOUT | ICC |
Write | L | L | X | DIN | ICC |

ABSOLUTE MAXIMUM RATINGS(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Power Supply Voltage Relative to GND</td>
<td>–0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td>VTERM</td>
<td>Terminal Voltage with Respect to GND</td>
<td>–0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>±20</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} )</td>
<td>Output HIGH Voltage</td>
<td>( V_{DD} = \text{Min.}, \ IOH = -2.0 \text{ mA} )</td>
<td>2.4</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output LOW Voltage</td>
<td>( V_{DD} = \text{Min.}, \ IOL = 4.0 \text{ mA} )</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input HIGH Voltage</td>
<td></td>
<td>2.2</td>
<td>( V_{DD} + 0.3 )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input LOW Voltage(^{(1)})</td>
<td></td>
<td>-0.3</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Leakage</td>
<td>( GND \leq V_{IN} \leq V_{DD} )</td>
<td>Com.</td>
<td>-1</td>
<td>1 ( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ind.</td>
<td>-2</td>
<td>2</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{LO} )</td>
<td>Output Leakage</td>
<td>( GND \leq V_{OUT} \leq V_{DD}, \text{ Outputs Disabled} )</td>
<td>Com.</td>
<td>-1</td>
<td>1 ( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ind.</td>
<td>-2</td>
<td>2</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

Notes:
1. \( V_{IL} \) (min.) = -0.3V (DC); \( V_{IL} \) (min.) = -2.0V (pulse width \( \leq \) 2.0 ns).
2. \( V_{IH} \) (max.) = \( V_{DD} + 0.5 \text{ V} \) (DC); \( V_{IH} \) (max.) = \( V_{DD} + 2.0 \text{ V} \) (pulse width \( \leq \) 2.0 ns).
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

---

### OPERATING RANGE

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temperature</th>
<th>Speed (ns)</th>
<th>( V_{DD} )(^{(1)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>10</td>
<td>3.3V, +10%, –5%</td>
</tr>
<tr>
<td>Industrial</td>
<td>–40°C to +85°C</td>
<td>10</td>
<td>3.3V + 10%, –5%</td>
</tr>
</tbody>
</table>

Note: 1. If operated at 12ns, \( V_{DD} \) range is 3.3V + 10%.

---

\(^{(1)}\) \( V_{DD} \) \( + \) 10% for Industrial at 12ns.
### POWER SUPPLY CHARACTERISTICS

**POWER SUPPLY CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Sym.</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>-10 ns</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc1</td>
<td>VDD Operating Supply Current</td>
<td>VDD = Max., CE = VIL</td>
<td>Com.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOUT = 0 mA, f = 1 MHz</td>
<td>Ind.</td>
<td>—</td>
</tr>
<tr>
<td>Icc2</td>
<td>VDD Dynamic Operating Supply Current</td>
<td>VDD = Max., CE = VIL</td>
<td>Com.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOUT = 0 mA, f = fMAX</td>
<td>Ind.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>typ. (2)</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>Isb1</td>
<td>TTL Standby Current (TTL Inputs)</td>
<td>VDD = Max., VIN = VH or VL, CE ≥ VH, f = 0</td>
<td>Com.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Ind.</td>
<td>—</td>
</tr>
<tr>
<td>Isb2</td>
<td>CMOS Standby Current (CMOS Inputs)</td>
<td>VDD = Max., VIN ≥ VDD – 0.2V, or VIL ≤ 0.2V, f = 0</td>
<td>Com.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CE ≥ VDD – 0.2V,</td>
<td>Ind.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>typ. (2)</td>
<td></td>
<td>2</td>
</tr>
</tbody>
</table>

**Notes:**
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at VDD = 3.3V, TA = 25°C and not 100% tested.

### CAPACITANCE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cin</td>
<td>Input Capacitance</td>
<td>VIN = 0V</td>
<td>6</td>
<td>pF</td>
</tr>
<tr>
<td>Cout</td>
<td>Output Capacitance</td>
<td>VOUT = 0V</td>
<td>5</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: TA = 25°C, f = 1 MHz, VDD = 3.3V.
**READ CYCLE SWITCHING CHARACTERISTICS**\(^{(1)}\) (Over Operating Range)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{RC})</td>
<td>Read Cycle Time</td>
<td>10</td>
<td>—</td>
<td>12</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{AA})</td>
<td>Address Access Time</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>12</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{OHA})</td>
<td>Output Hold Time</td>
<td>2</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{ACE})</td>
<td>CE Access Time</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>12</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{DOE})</td>
<td>OE Access Time</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LZOE}^{(2)})</td>
<td>OE to Low-Z Output</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{HZOE}^{(2)})</td>
<td>OE to High-Z Output</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LZCE}^{(2)})</td>
<td>CE to Low-Z Output</td>
<td>3</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{HZCE}^{(2)})</td>
<td>CE to High-Z Output</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PU}^{(3)})</td>
<td>CE to Power-Up</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PD}^{(3)})</td>
<td>CE to Power-Down</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>12</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

**AC TEST CONDITIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Level</td>
<td>0V to 3.0V</td>
</tr>
<tr>
<td>Input Rise and Fall Times</td>
<td>3 ns</td>
</tr>
<tr>
<td>Input and Output Timing and Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>See Figures 1 and 2</td>
</tr>
</tbody>
</table>

**AC TEST LOADS**

![Figure 1.](image1)

![Figure 2.](image2)
AC WAVEFORMS

READ CYCLE NO. 1\(^{(1,2)}\)

![AC Waveform Diagram 1](AC_Waveform_Diagram_1.png)

- DATA VALID
- PREVIOUS DATA VALID
- ADDRESS
- DOUT
- \(t_{RC}\)
- \(t_{AA}\)
- \(t_{OHA}\)

READ CYCLE NO. 2\(^{(1,3)}\)

![AC Waveform Diagram 2](AC_Waveform_Diagram_2.png)

- HIGH-Z
- DATA VALID
- ADDRESS
- DOUT
- \(t_{RC}\)
- \(t_{AA}\)
- \(t_{OHA}\)
- \(t_{DOE}\)
- \(t_{HZOE}\)
- \(t_{LZOE}\)
- \(t_{ACE}\)
- \(t_{HZCE}\)

Notes:
1. WE is HIGH for a Read Cycle.
2. The device is continuously selected. OE, CE = VIH.
3. Address is valid prior to or coincident with CE LOW transitions.
## WRITE CYCLE SWITCHING CHARACTERISTICS\(^{(1,2)}\) (Over Operating Range)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>-10 ns</th>
<th>-12 ns</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>( t_{WC} )</td>
<td>Write Cycle Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SCE} )</td>
<td>( \overline{CE} ) to Write End</td>
<td>8</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>( t_{AW} )</td>
<td>Address Setup Time to Write End</td>
<td>8</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>( t_{HA} )</td>
<td>Address Hold from Write End</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>( t_{SA} )</td>
<td>Address Setup Time</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>( t_{PWE1} )</td>
<td>( \overline{WE} ) Pulse Width ((\overline{OE} ) HIGH)</td>
<td>7</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>( t_{PWE2} )</td>
<td>( \overline{WE} ) Pulse Width ((\overline{OE} ) LOW)</td>
<td>10</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>( t_{SD} )</td>
<td>Data Setup to Write End</td>
<td>6.5</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>( t_{HD} )</td>
<td>Data Hold from Write End</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>( t_{HZWE} ) (^{(3)})</td>
<td>( \overline{WE} ) LOW to High-Z Output</td>
<td>—</td>
<td>3.5</td>
<td>—</td>
</tr>
<tr>
<td>( t_{LZWE} ) (^{(3)})</td>
<td>( \overline{WE} ) HIGH to Low-Z Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of \(\overline{CE} \) LOW and \(\overline{WE} \) LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

### AC WAVEFORMS

#### WRITE CYCLE NO. 1 (\(\overline{CE} \) Controlled, \(\overline{OE} \) is HIGH or LOW) \(^{(1)}\)
WRITE CYCLE NO. 2 (\(\text{WE} \) Controlled, \(\overline{\text{OE}}\) is HIGH During Write Cycle) \(^{(1,2)}\)

\[
\text{ADDRESS} \quad \text{VALID ADDRESS} \quad t_{WC} \quad t_{HA}
\]
\[
\overline{\text{OE}} \quad t_{PWE1} \quad t_{AW} \quad t_{SA} \quad t_{HZWE} \quad t_{LZWE}
\]
\[
\overline{\text{CE}} \quad \text{LOW}
\]
\[
\text{WE} \quad t_{PWE1} \quad t_{AW} \quad t_{HZWE} \quad t_{LZWE} \quad t_{SA} \quad t_{PWE2}
\]
\[
\text{DOUT} \quad \text{DATA UNDEFINED} \quad \text{HIGH-Z} \quad t_{SD} \quad t_{HD}
\]
\[
\text{DIN} \quad \text{DATAIN VALID}
\]

WRITE CYCLE NO. 3 (\(\text{WE} \) Controlled, \(\overline{\text{OE}}\) is LOW During Write Cycle) \(^{(1)}\)

\[
\text{ADDRESS} \quad \text{VALID ADDRESS} \quad t_{WC} \quad t_{HA}
\]
\[
\overline{\text{OE}} \quad \text{LOW}
\]
\[
\overline{\text{CE}} \quad \text{LOW}
\]
\[
\text{WE} \quad t_{PWE2} \quad t_{AW} \quad t_{HZWE} \quad t_{LZWE} \quad t_{SA} \quad t_{PWE2}
\]
\[
\text{DOUT} \quad \text{DATA UNDEFINED} \quad \text{HIGH-Z} \quad t_{SD} \quad t_{HD}
\]
\[
\text{DIN} \quad \text{DATAIN VALID}
\]

Notes:
1. The internal write time is defined by the overlap of \(\overline{\text{CE}}\) LOW and \(\overline{\text{WE}}\) LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if \(\overline{\text{OE}} > V_{\text{IH}}\).
**DATA RETENTION SWITCHING CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DR}$</td>
<td>$V_{DD}$ for Data Retention</td>
<td>See Data Retention Waveform</td>
<td>2.0</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DR}$</td>
<td>Data Retention Current</td>
<td>$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$</td>
<td>—</td>
<td>2</td>
<td>40</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$t_{SDR}$</td>
<td>Data Retention Setup Time</td>
<td>See Data Retention Waveform</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RDR}$</td>
<td>Recovery Time</td>
<td>See Data Retention Waveform</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
1. Typical Values are measured at $V_{DD} = 3.3V$, $T_a = 25^\circ C$ and not 100% tested.

**DATA RETENTION WAVEFORM (\overline{CE} Controlled)**

![Data Retention Waveform Diagram](image-url)
ORDERING INFORMATION

**Commercial Range: 0°C to +70°C**

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>IS61LV256AL-10T</td>
<td>TSOP - Type I</td>
</tr>
<tr>
<td></td>
<td>IS61LV256AL-10TL</td>
<td>TSOP - Type I, Lead-free</td>
</tr>
<tr>
<td></td>
<td>IS61LV256AL-10J</td>
<td>300-mil Plastic SOJ</td>
</tr>
<tr>
<td></td>
<td>IS61LV256AL-10JL</td>
<td>300-mil Plastic SOJ, Lead-free</td>
</tr>
</tbody>
</table>

ORDERING INFORMATION

**Industrial Range: –40°C to +85°C**

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>IS61LV256AL-10TI</td>
<td>TSOP - Type I</td>
</tr>
<tr>
<td></td>
<td>IS61LV256AL-10TLI</td>
<td>TSOP - Type I, Lead-free</td>
</tr>
<tr>
<td></td>
<td>IS61LV256AL-10JI</td>
<td>300-mil Plastic SOJ</td>
</tr>
<tr>
<td></td>
<td>IS61LV256AL-10JLI</td>
<td>300-mil Plastic SOJ, Lead-free</td>
</tr>
</tbody>
</table>
## Package Outline

### NOTE:

1. Controlling dimension: mm
2. Dimension D1 and E do not include mold protrusion.
3. Dimension E1 and D do not include dambar protrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm.
5. At the seating plane after mutilated.