IS65WV25616ALL
IS65WV25616BLL

256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC SRAM

FEATURES

• High-speed access time: 55ns, 70ns
• CMOS low power operation
  36 mW (typical) operating
  9 µW (typical) CMOS standby
• TTL compatible interface levels
• Single power supply
  1.65V--2.2V VDD (65WV25616ALL)
  2.5V--3.6V VDD (65WV25616BLL)
• Fully static operation: no clock or refresh required
• Three state outputs
• Data control for upper and lower bytes
• TEMPERATURE OFFERINGS:
  Option A1: -40°C to +85°C
  Option A2: -40°C to +105°C
  Option A3: -40°C to +125°C
• Lead-free available

DESCRIPTION

The ISSI IS65WV25616ALL/IS65WV25616BLL are high-speed, low power, 4M bit SRAMs organized as 256K words by 16 bits. It is fabricated using ISSI’s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1 is HIGH (deselected) or when CS1 is LOW, and both LB and UB are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE) controls both writing and reading of the memory. A data byte allows Upper Byte (UB) and Lower Byte (LB) access.

The IS65WV25616BALL/65WV25616BLL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II) and 48-pin mini BGA (6mmx8mm).

FUNCTIONAL BLOCK DIAGRAM

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a) the risk of injury or damage has been minimized;
b) the user assume all such risks; and

c) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances.
PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A17</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>I/O0-I/O15</td>
<td>Data Inputs/Outputs</td>
</tr>
<tr>
<td>CS1</td>
<td>Chip Enable Input</td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable Input</td>
</tr>
<tr>
<td>WE</td>
<td>Write Enable Input</td>
</tr>
<tr>
<td>LB</td>
<td>Lower-byte Control (I/O0-I/O7)</td>
</tr>
<tr>
<td>UB</td>
<td>Upper-byte Control (I/O8-I/O15)</td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
</tr>
<tr>
<td>VDD</td>
<td>Power</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

PIN CONFIGURATIONS

48-ball mini BGA (6mm x 8mm)
(Package Code B)

44-Pin mini TSOP (Type II)
2 Chip Enable Option
(Package Code T2)
## TRUTH TABLE

<table>
<thead>
<tr>
<th>Mode</th>
<th>WE</th>
<th>CS1</th>
<th>OE</th>
<th>LB</th>
<th>UB</th>
<th>I/O0-I/O7</th>
<th>I/O8-I/O15</th>
<th>VDD Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not Selected</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Isb1, Isb2</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Isb1, Isb2</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Isb1, Isb2</td>
</tr>
<tr>
<td>Output Disabled</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Icc</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Icc</td>
</tr>
<tr>
<td>Read</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>DOUT</td>
<td>High-Z</td>
<td>Icc</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>High-Z</td>
<td>DOUT</td>
<td>Icc</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>DOUT</td>
<td>DOUT</td>
<td></td>
</tr>
<tr>
<td>Write</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>DIN</td>
<td>High-Z</td>
<td>Icc</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>H</td>
<td>L</td>
<td>High-Z</td>
<td>DIN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>DIN</td>
<td>DIN</td>
<td></td>
</tr>
</tbody>
</table>
### DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>V_{dd}</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{VIH} )</td>
<td>Input HIGH Voltage</td>
<td>( \text{IOH} = -0.1 \text{ mA} )</td>
<td>1.65-2.2V</td>
<td>1.4</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{IOH} = -1 \text{ mA} )</td>
<td>2.5-3.6V</td>
<td>2.2</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>( \text{VIL} )</td>
<td>Output LOW Voltage</td>
<td>( \text{IOL} = 0.1 \text{ mA} )</td>
<td>1.65-2.2V</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{IOL} = 2.1 \text{ mA} )</td>
<td>2.5-3.6V</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>( \text{VIH} )</td>
<td>Input HIGH Voltage</td>
<td></td>
<td>1.65-2.2V</td>
<td>1.4</td>
<td>( \text{VDD} + 0.2 )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5-3.6V</td>
<td>2.2</td>
<td>( \text{VDD} + 0.3 )</td>
<td>V</td>
</tr>
<tr>
<td>( \text{VIL} )</td>
<td>Input LOW Voltage</td>
<td></td>
<td>1.65-2.2V</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5-3.6V</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td>( \text{IIL} )</td>
<td>Input Leakage</td>
<td>( \text{GND} \leq \text{VIN} \leq \text{VDD} )</td>
<td>—2</td>
<td>2</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td>( \text{ILO} )</td>
<td>Output Leakage</td>
<td>( \text{GND} \leq \text{VOUT} \leq \text{VDD}, \text{Outputs Disabled} )</td>
<td>—2</td>
<td>2</td>
<td>—</td>
<td>μA</td>
</tr>
</tbody>
</table>

**Notes:**
1. \( \text{VIL} \) (min.) = \(-1.0\)V for pulse width less than 10 ns.
### IS65WV25616ALL, POWER SUPPLY CHARACTERISTICS

*(Over Operating Range)*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Max.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>VDD Dynamic Operating Supply Current</td>
<td>VDD = Max., IOUT = 0 mA, f = fMAX</td>
<td>A1</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2, A3</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>ICC1</td>
<td>Operating Supply Current</td>
<td>VDD = Max., CS1 = 0.2V, WE = VDD-0.2V, f = 1 MHz</td>
<td>A1</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2, A3</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>Isb1</td>
<td>TTL Standby Current (TTL Inputs)</td>
<td>VDD = Max., V_IN = V_H or V_L, CS1 = V_H, f = 1 MHz</td>
<td>A1</td>
<td>0.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2, A3</td>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ULB Control</td>
<td>VDD = Max., V_IN = V_H or V_L, CS1 = V_L, f = 0, UB = V_H, LB = V_H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isb2</td>
<td>CMOS Standby Current (CMOS Inputs)</td>
<td>VDD = Max., CS1 ≥ VDD – 0.2V, V_IN ≥ VDD – 0.2V or V_IN ≤ 0.2V, f = 0</td>
<td>A1</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ULB Control</td>
<td>VDD = Max., CS1 = V_L, V_IN ≤ 0.2V, f = 0, UB / LB = VDD – 0.2V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### IS65WV25616BLL, POWER SUPPLY CHARACTERISTICS

*(Over Operating Range)*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Max.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>VDD Dynamic Operating Supply Current</td>
<td>VDD = Max., IOUT = 0 mA, f = fMAX</td>
<td>A1</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2, A3</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>ICC1</td>
<td>Operating Supply Current</td>
<td>VDD = Max., CS1 = 0.2V, WE = VDD-0.2V, f = 1 MHz</td>
<td>A1</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2, A3</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Isb1</td>
<td>TTL Standby Current (TTL Inputs)</td>
<td>VDD = Max., V_IN = V_H or V_L, CS1 = V_H, f = 1 MHz</td>
<td>A1</td>
<td>0.45</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2, A3</td>
<td>0.45</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ULB Control</td>
<td>VDD = Max., V_IN = V_H or V_L, CS1 = V_L, f = 0, UB = V_H, LB = V_H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isb2</td>
<td>CMOS Standby Current (CMOS Inputs)</td>
<td>VDD = Max., CS1 ≥ VDD – 0.2V, V_IN ≥ VDD – 0.2V or V_IN ≤ 0.2V, f = 0</td>
<td>A1</td>
<td>20</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td></td>
<td></td>
<td>90</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ULB Control</td>
<td>VDD = Max., CS1 = V_L, V_IN ≤ 0.2V, f = 0, UB / LB = VDD – 0.2V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**CAPACITANCE**(1)  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>VIN = 0V</td>
<td>8</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Input/Output Capacitance</td>
<td>VOUT = 0V</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Note:**  
1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>IS65WV25616ALL (Unit)</th>
<th>IS65WV25616BLL (Unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Level</td>
<td>0.4V to VDD-0.2V</td>
<td>0.4V to VDD-0.3V</td>
</tr>
<tr>
<td>Input Rise and Fall Times</td>
<td>5 ns 5ns</td>
<td></td>
</tr>
<tr>
<td>Input and Output Timing and Reference Level</td>
<td>VREF VREF</td>
<td></td>
</tr>
<tr>
<td>Output Load</td>
<td>See Figures 1 and 2</td>
<td>See Figures 1 and 2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IS65WV25616ALL</th>
<th>IS65WV25616BLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.65V-2.2V</td>
<td>2.5V - 3.6V</td>
</tr>
<tr>
<td>R1(Ω)</td>
<td>3070</td>
</tr>
<tr>
<td>R2(Ω)</td>
<td>3150</td>
</tr>
<tr>
<td>VREF</td>
<td>0.9V 1.5V</td>
</tr>
<tr>
<td>VTM</td>
<td>1.8V 2.8V</td>
</tr>
</tbody>
</table>

**AC TEST LOADS**

![Figure 1](62WV5126ALL_tst1a.png)  
![Figure 2](25616I_tst1c.png)
## READ CYCLE SWITCHING CHARACTERISTICS

### (Over Operating Range)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>55 ns</th>
<th>70 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>(\text{trc})</td>
<td>Read Cycle Time</td>
<td>55</td>
<td>—</td>
</tr>
<tr>
<td>(\text{tAA})</td>
<td>Address Access Time</td>
<td>—</td>
<td>55</td>
</tr>
<tr>
<td>(\text{toha})</td>
<td>Output Hold Time</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>(\text{tacs1})</td>
<td>CS1 Access Time</td>
<td>—</td>
<td>55</td>
</tr>
<tr>
<td>(\text{tdoe})</td>
<td>OE Access Time</td>
<td>—</td>
<td>25</td>
</tr>
<tr>
<td>(\text{tHZOE}^{(2)})</td>
<td>OE to High-Z Output</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>(\text{tlzoe}^{(2)})</td>
<td>OE to Low-Z Output</td>
<td>5</td>
<td>—</td>
</tr>
<tr>
<td>(\text{tHZCS1})</td>
<td>CS1 to High-Z Output</td>
<td>0</td>
<td>20</td>
</tr>
<tr>
<td>(\text{tlzcs1})</td>
<td>CS1 to Low-Z Output</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>(\text{tBA})</td>
<td>LB, UB Access Time</td>
<td>—</td>
<td>55</td>
</tr>
<tr>
<td>(\text{tHZB})</td>
<td>LB, UB to High-Z Output</td>
<td>0</td>
<td>20</td>
</tr>
<tr>
<td>(\text{tlzB})</td>
<td>LB, UB to Low-Z Output</td>
<td>0</td>
<td>—</td>
</tr>
</tbody>
</table>

### Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
AC WAVEFORMS

READ CYCLE NO. 1\(^{(1,2)}\) (Address Controlled) (\(\overline{CS1} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}, \overline{UB} \text{ or } \overline{LB} = V_{IL}\))

[Diagram of AC waveforms for READ CYCLE NO. 1]

READ CYCLE NO. 2\(^{(1,3)}\) (\(\overline{CS1}, \overline{OE}, \text{ AND } \overline{UB}/\overline{LB} \text{ Controlled})

[Diagram of AC waveforms for READ CYCLE NO. 2]

Notes:
1. \(\overline{WE}\) is HIGH for a Read Cycle.
2. The device is continuously selected. \(\overline{OE}, \overline{CS1}, \overline{UB}, \text{ or } \overline{LB} = V_{IL}, \overline{WE} = V_{IH}.
3. Address is valid prior to or coincident with \(CS1\) LOW transition.
WRITE CYCLE SWITCHING CHARACTERISTICS\(^{(1,2)}\) (Over Operating Range)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>55 ns</th>
<th>70 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>(t_{WC})</td>
<td>Write Cycle Time</td>
<td>55</td>
<td>—</td>
</tr>
<tr>
<td>(t_{CS1})</td>
<td>CS1 to Write End</td>
<td>45</td>
<td>—</td>
</tr>
<tr>
<td>(t_{AW})</td>
<td>Address Setup Time to Write End</td>
<td>45</td>
<td>—</td>
</tr>
<tr>
<td>(t_{HA})</td>
<td>Address Hold from Write End</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>(t_{SA})</td>
<td>Address Setup Time</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>(t_{PW})</td>
<td>LB, UB Valid to End of Write</td>
<td>45</td>
<td>—</td>
</tr>
<tr>
<td>(t_{PWE})</td>
<td>WE Pulse Width</td>
<td>40</td>
<td>—</td>
</tr>
<tr>
<td>(t_{SD})</td>
<td>Data Setup to Write End</td>
<td>25</td>
<td>—</td>
</tr>
<tr>
<td>(t_{HD})</td>
<td>Data Hold from Write End</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>(t_{HZWE})(3)</td>
<td>WE LOW to High-Z Output</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>(t_{LZWE})(3)</td>
<td>WE HIGH to Low-Z Output</td>
<td>5</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of CS1 LOW and UB or LB, and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
AC WAVEFORMS

WRITE CYCLE NO. 1\(^{(1,2)}\) \( (\overline{CS1} \text{ Controlled}, \overline{OE} = \text{HIGH or LOW})\)

Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \(CS1, WE\) inputs and at least one of the \(LB\) and \(UB\) inputs being in the LOW state.
2. \(WRITE = (CS1) \land (LB) = (UB) \land (WE)\).

WRITE CYCLE NO. 2 \( (WE \text{ Controlled; } OE \text{ is HIGH During Write Cycle})\)
WRITE CYCLE NO. 3 (WE Controlled; OE is LOW During Write Cycle)

WRITE CYCLE NO. 4 (UB/LB Controlled)
DATA RETENTION SWITCHING CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDR</td>
<td>$V_{DD}$ for Data Retention</td>
<td>See Data Retention Waveform</td>
<td>1.2</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>IDR</td>
<td>Data Retention Current</td>
<td>$V_{DD} = 1.2V, , CS1 \geq V_{DD} - 0.2V$</td>
<td>A1</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A2</td>
<td>—</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A3</td>
<td>—</td>
<td>60</td>
</tr>
<tr>
<td>tSDR</td>
<td>Data Retention Setup Time</td>
<td>See Data Retention Waveform</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRDR</td>
<td>Recovery Time</td>
<td>See Data Retention Waveform</td>
<td>$t_{HC}$</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

DATA RETENTION WAVEFORM (CS1 Controlled)

![Data Retention Waveform Diagram](51216LT_DR.eps)
ORDERING INFORMATION: IS65WV25616ALL (1.65V-2.2V)

Temperature Range (A1): –40°C to +85°C

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>IS65WV25616ALL-70CTLA1</td>
<td>44-pin TSOP-II, Copper Leadframe, Lead-free</td>
</tr>
</tbody>
</table>

Temperature Range (A2): –40°C to +105°C

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>IS65WV25616ALL-70CTLA2</td>
<td>44-pin TSOP-II, Copper Leadframe, Lead-free</td>
</tr>
</tbody>
</table>

Temperature Range (A3): –40°C to +125°C

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>IS65WV25616ALL-70CTLA3</td>
<td>44-pin TSOP-II, Copper Leadframe, Lead-free</td>
</tr>
</tbody>
</table>

ORDERING INFORMATION: IS65WV25616BLL (2.5V-3.6V)

Temperature Range (A1): –40°C to +85°C

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>55</td>
<td>IS65WV25616BLL-55CTLA1</td>
<td>44-pin TSOP-II, Copper Leadframe, Lead-free</td>
</tr>
<tr>
<td></td>
<td>IS65WV25616BLL-55BA1</td>
<td>48-ball BGA</td>
</tr>
<tr>
<td></td>
<td>IS65WV25616BLL-55BLA1</td>
<td>48-ball BGA, Lead-free</td>
</tr>
</tbody>
</table>

Temperature Range (A2): –40°C to +105°C

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>IS65WV25616BLL-70CTLA2</td>
<td>44-pin TSOP-II, Copper Leadframe, Lead-free</td>
</tr>
<tr>
<td></td>
<td>IS65WV25616BLL-70BA2</td>
<td>48-ball BGA</td>
</tr>
<tr>
<td></td>
<td>IS65WV25616BLL-70BLA2</td>
<td>48-ball BGA, Lead-free</td>
</tr>
</tbody>
</table>

Temperature Range (A3): –40°C to +125°C

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Order Part No.</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>IS65WV25616BLL-70CTLA3</td>
<td>44-pin TSOP-II, Copper Leadframe, Lead-free</td>
</tr>
<tr>
<td></td>
<td>IS65WV25616BLL-70BA3</td>
<td>48-ball BGA</td>
</tr>
<tr>
<td></td>
<td>IS65WV25616BLL-70BLA3</td>
<td>48-ball BGA, Lead-free</td>
</tr>
</tbody>
</table>
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DIMENSION IN MM</th>
<th>DIMENSION IN INCH</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.00 1.20 0.039</td>
<td>0.047</td>
</tr>
<tr>
<td>A1</td>
<td>0.05 0.15 0.002</td>
<td>0.006</td>
</tr>
<tr>
<td>A2</td>
<td>0.95 1.00 0.037 0.039 0.041</td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>0.30 0.45 0.012</td>
<td>0.018</td>
</tr>
<tr>
<td>D</td>
<td>18.28 18.41 18.54 0.720 0.725 0.730</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>11.56 11.76 11.96 0.455 0.463 0.471</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>10.03 10.16 10.29 0.395 0.400 0.405</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>0.80 BSC. 0.031 BSC.</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.40 0.69 0.016 0.027</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>0.25 BSC. 0.010 BSC.</td>
<td></td>
</tr>
<tr>
<td>ZD</td>
<td>0.805 REF. 0.032 REF.</td>
<td></td>
</tr>
<tr>
<td>ø</td>
<td>0 8° 0 8°</td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
- DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
NOTE:

1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-207

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DIMENSION IN MM</th>
<th>DIMENSION IN INCH</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.20</td>
<td>0.047</td>
</tr>
<tr>
<td>A1</td>
<td>0.30 0.35 0.40</td>
<td>0.008 0.012 0.016</td>
</tr>
<tr>
<td>φA0</td>
<td>0.30 0.35 0.40</td>
<td>0.008 0.012 0.016</td>
</tr>
<tr>
<td>D</td>
<td>7.90 8.00 8.10</td>
<td>0.311 0.315 0.319</td>
</tr>
<tr>
<td>D1</td>
<td>5.25 BSC</td>
<td>0.207 BSC</td>
</tr>
<tr>
<td>E</td>
<td>5.90 6.00 6.10</td>
<td>0.2320.2360.240</td>
</tr>
<tr>
<td>E1</td>
<td>3.75 BSC</td>
<td>0.148 BSC</td>
</tr>
<tr>
<td>e</td>
<td>0.75 BSC</td>
<td>0.030 BSC</td>
</tr>
<tr>
<td>ZD</td>
<td>1.375 REF.</td>
<td>0.054 REF.</td>
</tr>
<tr>
<td>ZE</td>
<td>1.125 REF.</td>
<td>0.044 REF.</td>
</tr>
</tbody>
</table>