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4Mbit ADMUX SRAM

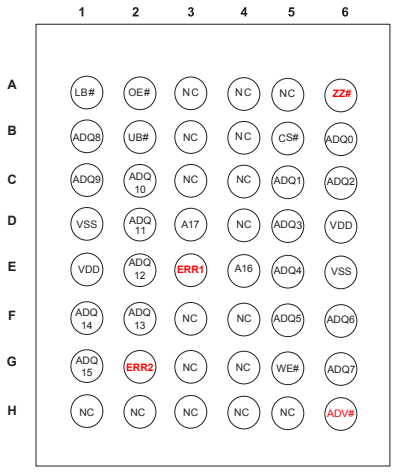
256Kx16 HIGH SPEED ECC ASYNCHRONOUS CMOS STATIC RAM with MUXED ADDRESS & DATA

KEY FEATURES:

- High-speed access time: 10ns, 12ns, 18ns
- Single power supply
  –2.4V-3.6V VDD
- Ultra Low Standby Current with ZZ# pin
  -IZZ = 30µA (typ.)
- Error Detection and Correction per individual 8-bits (1 Byte) with optional ERR1/ERR2 output pins:
  -ERR1 pin indicates 1-bit error detection and correction.
  -ERR2 pin indicates multi-bit error detection
- ADMUX inputs/outputs: ADQ0~ADQ15.
- Industrial and Automotive temperature support
- Lead-free available

BGA PINOUT:

48-Pin mini BGA (6mm x 8mm) with ZZ# and ERR1/2



DESCRIPTION:

The ISSI IS61/64WV25616MEBLL are high-speed, low power, 4M bit ADMUX static RAMs organized as 256K words by 16 bits. It is fabricated using ISSI's high-performance CMOS technology and features ECC function to improve reliability.

Our highly reliable process coupled with innovative circuit design techniques including ECC (SECDED: Single Error Correction Double Error Detection) yields high-performance and highly reliable devices.

When CS# is High (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Device is designed with a Ultra Low Standby Power option using Snooze mode when ZZ# is Low.

ADV# pin enables Address Path (ADQ=Address Buffer) by asserting ADV# input Low.
When ADV# is High, Data Path is enabled (ADQ=I/O Buffer) and the device can be used as an Asynchronous SRAM.

This ADMUX SRAM can reduce number of signal lines by sharing I/O signal lines with Address input signals.

The IS61/64WV25616MEBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm), and 44-pin TSOP (TYPE II).

Serving Major Market Segments with Quality and Long-Term Support

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IS61WV25616MEBLL
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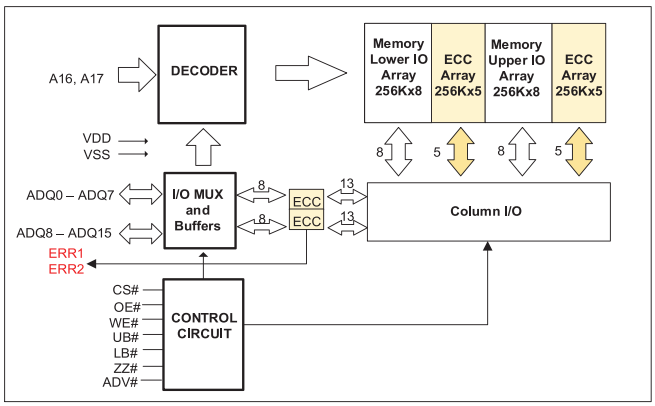
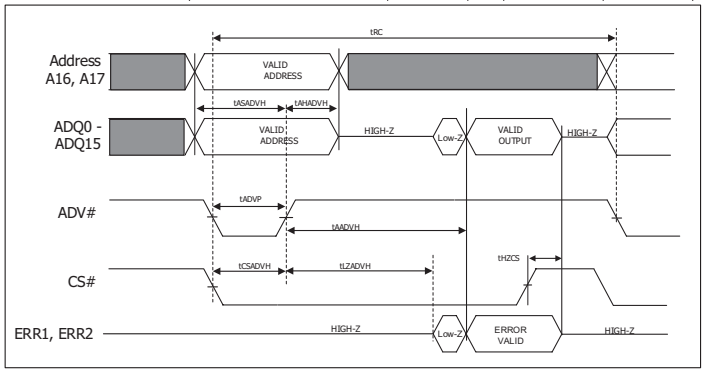
FUNCTIONAL BLOCK DIAGRAM:



TIMING DIAGRAM:

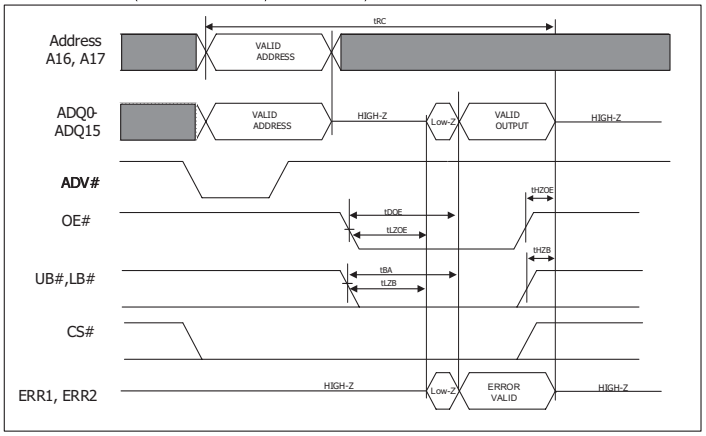
READ CYCLE NO. 1 [1,2,3] (ADV# AND CS# CONTROLLED, OE# , UB#, LB# = LOW , WE# = HIGH)



Notes:
1. ERR1, ERR2 signals act like a Read Data Q during Read Operation.
2. ADQ bus must be entered into HIGH-Z state at the end of the READ cycle by disabling OE#, CS#, or UB#/LB# to avoid bus contention with following external address.

TIMING DIAGRAM:

READ CYCLE NO. 2 (OE# CONTROLLED , WE# = HIGH)



TIMING DIAGRAM:

WRITE CYCLE NO. 1 (WE# CONTROLLED, UB#, LB# = LOW, OE# = HIGH)