For the case of constant failure rate ($\lambda(t)$ = constant), $R(t) = \exp(-\lambda t)$, $F(t) = 1 - \exp(-\lambda t)$ and $f(t) = dF(t)/dt = \lambda \exp(-\lambda t)$

$$\mathrm{MTTF} = \int_0^\infty t f(t)dt = \int_0^\infty t\lambda \exp(-\lambda t)dt = \frac{1}{\lambda_{use}}$$

where the point estimate of the failure rate at use conditions is calculated as:

$$\lambda_{use} = \frac{\lambda_{stress}}{AF_t \times AF_v}$$

New Product/Process Qualification

The products used for reliability testing are representative of all device families, package families, foundry locations, and assembly locations. The standards referenced by ISSI are JEDEC Standard 22 and MIL-STD-883, which have been universally used throughout the semiconductor industry.

Reliability is defined as the probability that a semiconductor device will perform its required function under the specified conditions for a stated period of time. The probability of survival prior to time t, R(t), plus the probability of failure, F(t), is always unity. Expressed as a formula:

R(t) + F(t) = 1, or R(t) = 1- F(t)

The probability of survival and failure is derived from the observed results of actual stress tests performed on the devices. High Temperature Operating Life (HTOL) will determine the expected failure rate, λ(t), under operating conditions. The other reliability tests, which are described in below, accelerate other expected conditions and contribute further survival /failure rates for both die/process and package.

1.1 Die/Process Reliability Tests

1) High Temperature Operating Life Test (HTOL)

(Refer to JEDEC 22-A108)

High temperature operating life test is performed to accelerate failure mechanisms that are activated by temperature while under bias. This test is used to predict long-term failure rates since acceleration by temperature is understood and the calculation for acceleration factor is well established. Prior to HTOL, all test samples are screened to standard electrical tests at low temperature and high temperature with prior burn-in. Dynamic operating conditions are applied to most cases and the test circuit is depending on the specific device. The typical stress voltage is 1.1 times of normal operating voltage. Unless otherwise specified, the stress temperature is maintained at 125 ℃. Devices are tested at prescribed

time-points. Failure rates are calculated in terms of FITs (failures in time). Each FIT represents one failure in 109 device-hours.

2) Infant Mortality (IM)

Infant mortality testing determines the early failure rate of a specific product and process. The test conditions are basically the same as the high temperature operating life test with an increased sample size to ensure an accurate failure rate. The test temperatures **Tj** can be set between 125 ℃to 150 ℃, depending on product type and the test environment. The typical stress voltage is at least 1.2 times of normal operating voltage. The failure rate data is used to determine a product burn-in strategy for each product and provide information for process improvement.

3) Electrostatic Discharge (ESD)

(Refer to ANSI/ESDA/JEDEC JS-001 and JS-002)

Electrostatic discharge sensitivity (ESD) tests are designed to measure the sensitivity of each device with respect to electrostatic discharges that may occur during device handling. Various test methods have been devised to analyze ESD. Currently, ISSI evaluate ESD using the following test methods. The human body model (HBM) is in accordance with the standard specified by ANSI/ESDA/JEDEC JS-001 while the charge device model (CDM) is by ANSI/ESDA/JEDEC JS-002.

The human body model is based on a high-voltage pulse (positive and negative) of longer duration, simulating discharge through human contact. The charge device model is based on the phenomenon where the semiconductor device itself carries a charge or where the charge induced to the device from charged object near the device is discharged. It reproduces the discharge mechanism in the form closest to the discharge phenomenon occurring in the field.

4) Latch-up

(Refer to JEDEC standard No. 78)

The latch-up test is designed specifically for CMOS processed devices to detect parasitic bipolar circuits that, when activated, may short power and ground nodes. Test conditions are significantly worse than normal operation variations to provide a margin for safe operation. Presently, ISSI evaluates latch-up based on JEDEC standard No. 78. For JEDEC standard, current (positive and negative) is injected into individual input/output pins in steps while the power supply current is monitored. The current into the test pin must rise to a minimum of 100 mA without a latch-up condition.

5) Soft Error Rate

(Refer to JEDEC Standard 89)

Semiconductor memory defects that can be recovered by rewriting the data are called soft errors. In addition to being caused by the power supply line and ground line noise, soft error are also caused by α-rays emitted from the trace amounts of uranium, thorium and other radioactive substances contained in the package or wiring materials.

There are two methods for evaluating soft errors: system tests which consist of actually operating large number of samples, and accelerated tests using a α-ray source.

When evaluating the absolute soft error value it is necessary to conduct system tests. However, system tests require many samples and long times (typically, 1000 samples and 1000 hours or more).

In contrast, accelerated tests allow evaluation in a short time, but have the problem that it is difficult to accurately obtain accelerated characteristics for a market environment.

Soft error rates are expressed in FIT units:

1 FIT = 1 Failure/109 Device-hours

6) Endurance Cycling

(Refer to MIL-STD-883 1033, JEDEC 22- A117)

The test is used to evaluate the quality of the tunnel oxide of Flash products. Continued program-erase operation can cause charge trapping or even breakdown in the tunnel oxide, resulting in threshold shift and eventually failure of a cell to retain data. The test requires typical 100k cycles at room temperature and high temperature. Large electrical field changes between the gate and drain of the memory cell can also cause damage of the oxide layer.

7) Data retention

(Refer to JEDEC 22- A117, JESD 47)

The test is to measure the stability of electron in the floating gate of Flash products. Devices are exposed to high temperature, typically, 125 or 150 ℃, which causes acceleration of charge loss or gain, resulting in shifting of threshold voltage. No bias is needed for this test. Charge trapping or defect in tunnel oxide and other dielectric, mobile ion contamination may contribute to the degrading of data retention performance.

8) High Temperature Storage Life Test (HTSL)

(Refer to JEDEC 22-A103)

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). Unless otherwise specified, the stress temperature is maintained at 150 ℃.

1.2 Package Reliability Tests

1) Highly Accelerated Stress Test (HAST)

(Refer to JEDEC 22 - A110)

The highly accelerated stress test provides constant multiple stress conditions including temperature, humidity, pressure, and voltage bias. It is performed for the purpose of evaluating the reliability of non-hermetic packaged devices operating in the humid environments. The multiple stress conditions accelerate the penetration of moisture through the package mold compound or along the interface between the external protective materials and the metallic conductors passing through package. When moisture reaches the die surface, the applied potential establishes an electrolytic condition that corrodes aluminum conductors and affects DC parameters of the device. Presence of contaminants on the die surface such as chlorine greatly accelerates the corrosion process. Additionally, excessive phosphorus in the passivation will react under these conditions.

2) Unbiased Autoclave (Pressure Cooker Test)

(Refer to JEDEC 22- A102)

The autoclave test is performed to evaluate the moisture resistance of non-hermetic packaged units. Devices are subject to pressure, humidity, and elevated temperature to accelerate the penetration of moisture through the molding compound or along the interface of the device pins and molding compound. Expected failure mechanisms include mobile ionic contamination, leakage along the die surface, or metal corrosion caused by reactive agents present on the die surface. The autoclave test is performed in a pressure chamber capable of maintaining temperature and pressure. Steam is introduced into the chamber until saturation, then the chamber is sealed and the temperature is elevated to 121 ℃, corresponding to a pressure of 30 psia (2 atm). This condition is maintained for the duration of the test. Upon completion of the specified time, the devices are cooled, dried and electrically tested. (Note: PCT is not applied for organic substrate package.)

3) Temperature Cycling Test (TCT)

(Refer to JEDEC 22- A104)

Temperature cycling test accelerates the effects that changes in the temperature will cause damage between different components within the specific die and packaging system due to different thermal expansion coefficients. Typical examples of damage caused by this test include package cracking, cracking or cratering of the die, passivation or metal de-lamination, and more subtle damage resulting impaired electrical performance. During testing devices are inserted into a chamber where the interior is cycled between specified temperatures and held at each temperature for a minimum of one minute. Temperature extremes depend on the condition selected in the test method. The total stress corresponds to the number of cycles completed at the specified temperature.

4)High Temperature Storage Life Test (HTSL)

(Refer to JEDEC 22-A103)

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). Unless otherwise specified, the stress temperature is maintained at 150 ℃.

5) Preconditioning Test (Moisture Sensitivity)

(Refer to JEDEC 22- A113 , J-STD-020)

Surface mount packages may be damaged during the solder reflow process when moisture in the package expands rapidly. Two test methods are utilized to determine which packages may be sensitive and what level of sensitivity exists. JEDEC test method A113 establishes the reliability of devices exposed to a specified preconditioning process at various moisture levels by subjecting preconditioned devices to HAST, PCT and TCT. The test result determines whether dry packing is necessary to ensure the reliability of the product after the assembly process.

6) Solderability

(Refer to J-STD-002)

The solderability test is used to determine the ability of package leads wetted by solder. This test verifies that the method of lead treatment to facilitate solderability is satisfactory and will allow successful solder connection to designated surface. (A) For Lead Frame package, the test is accomplished by immersing leads in flux then dipping the leads into molten solder of 215℃ ± 5℃ for non Pb free or 245℃±5 ℃for Pb free. No less than 95% coverage of the dipped area should be shown on each lead. (B) For Substrate package, the reflow temperature IR Reflow Soldering is Pb-free: 230~245℃ and SnPb: 215~230℃.

7) Mark Permanency

(Refer to JEDEC 22-B107)

The mark permanency test subject's package marking to solvents and cleaning solution commonly used for removing solder flux on circuit boards to ensure the marking will not become illegible. Devices and a brush are immersed into one of three specified solvents for one minute, and then removed. The devices are then brushed ten strokes. This process is repeated three times for each group of solvents and devices. After they are rinsed and dried, the devices are examined for legibility according to specified criteria.

8) Lead Integrity

(Refer to JEDEC 22-B105)

The lead integrity test provides tests for determining the integrity of devices leads, welds and seals. Devices are subject to various stresses including tension, bending fatigue and torque appropriate to the type of lead. Devices are then examined under optical microscope to determine any evidence of breakage, loosening or motion between the terminal and device body.

9) Solder Ball Shear

(Refer to JEDEC 22-B117)

This test method is used to assess the ability of solder balls to withstand mechanical shear forces that may be applied during device manufacturing, handling, test, shipment, and end-use conditions.

10) Bond Pull and Shear

(Refer to MIL-STD-883, Method 2011)

The purpose of these tests is to measure bond strength, evaluate bond strength/bond strength distributions or determine compliance with specified bond strength requirements of the applicable acquisition document.

Qualification Test Method and Acceptance Criteria

The summary shown in following tables give brief descriptions of the various reliability tests. Not all of the tests listed are performed on each product and other tests can be performed when appropriate.

Table 1: Qualification Test Method and Acceptance Criteria

	Test item	Applied with	Test method	Test condition	Sample #(Min) x lot	Acc No	Comments
1	HTOL High Temp. Operating Life	All ISSI products.	JEDEC 22 A108 MIL-STD-883 1005	T=125℃, Apply Voltage ≧Vcc max, Dynamic	77x3	0	Acceptable number is upon sample size. For Memory: Target failure rate < 100 FITs at 60% CL after 1 Khrs.
2	ESD Electrostatic Discharge	All ISSI products.	ANSI/ESDA/JEDEC JS-001 ANSI/ESDA/JEDEC JS-002	Human Body Model (HBM) R=1.5kohm, C=100pF. Charge Device Model (CDM).	3x1 HBM 3x1 CDM	0 0	3 samples for each test mode HBM ≧ ±2000V. CDM≧±500V (corner pins >= ±750V) for SRAM/DRAM Automotive devices 3pcs for each voltage level for Analog