

Application Note

So far, the smallest DDR2 SDRAM available has been 256Mb organized as 16Mx16. Many embedded applications such as found in networking, automotive and industrial / medical markets require 32 bit wide data buses. In application that only required 8M address space, engineers have been limited to using larger memories (16M) than required producing a sub-optimal design.

ISSI has recently announced the first 256Mb DDR2 SDRAM with a 32-bit bus. The purpose of this application note is a quick reference showing how to replace two 16Mx16 DDR2 SDRAMs with a single 8Mx32 DDR2 SDRAM using the IS43DR32800A or IS43DR32801A.

Figure 1 shows a typical connection between a 32-bit DDR2 DRAM controller as often implemented in a FPGA or a 32-bit microprocessor or single-chip DSP.

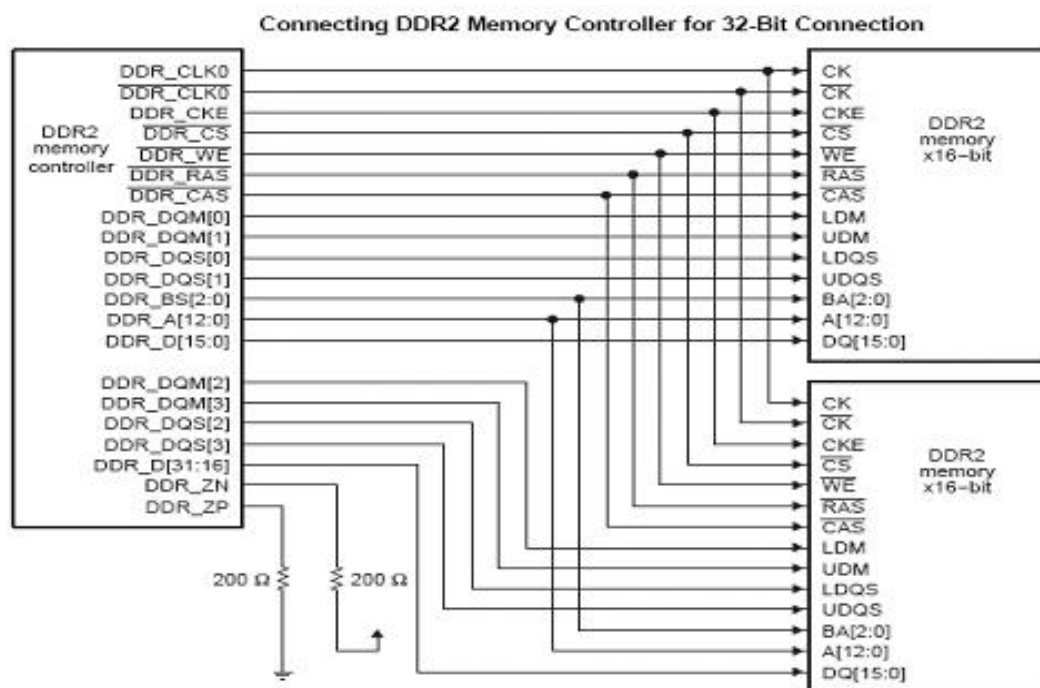


Fig. 1: 32-bit bus by using two 16Mx16 DDR2-SDRAM

Figure 2 shows this same design using a single “x32 DDR2 SDRAM”. The advantages of a single “x32 DDR2 SDRAM” offers include reduced PCB area, fewer package balls, lower power consumption, reduced system cost, and enhanced reliability and performance.

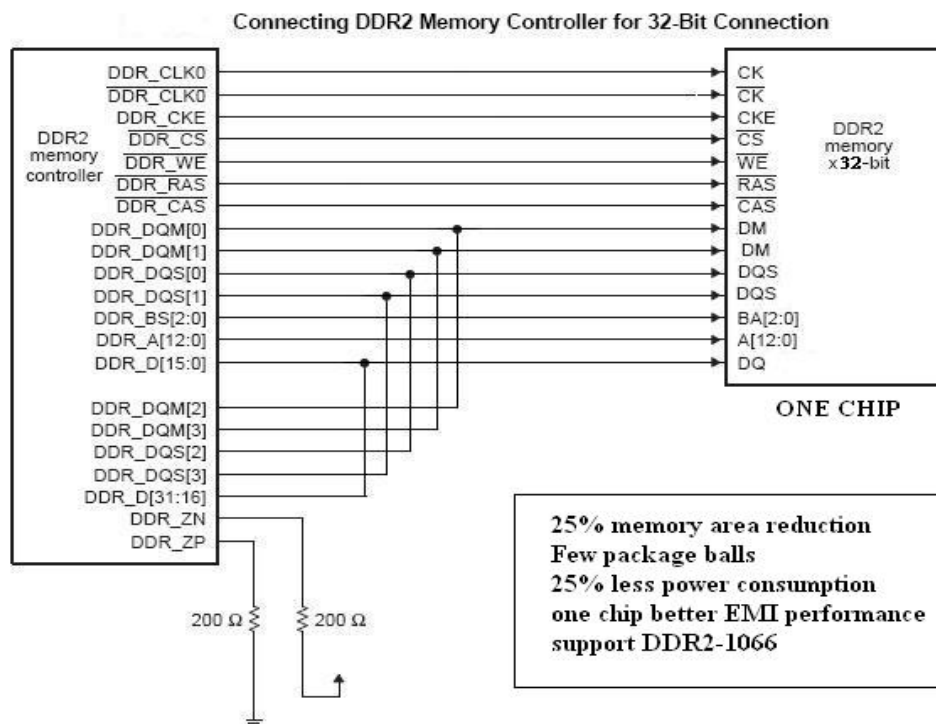


Fig. 2: 32-bit bus by using one 8Mx32 IS43DR32800A

One of the most popular families of single-chip DSPs is the TMS320 series from Texas Instruments. The section below provides a quick reference on how to set the DRAM controller within the DSP to interface to the ISSI 8Mx32 DDR2 SDRAM.

In Figure 3, the register setting for supporting an 8Mx32 DDR2 are shown. The IS43DR32800A has a 512 word page size while the IS32DR328001A has a 256 word page size.

Controller vendor:

1. TMS320DM644X from Texas Instruments.

Modify setting of the SDRAM BANK Configuration Register, Page 41

Bit	Field	Value	Description
11-9	CL	0-7h 0-1h 2h 3h 4h 5h 6h-7h	CAS latency. Reserved CAS latency of 2 CAS latency of 3 CAS latency of 4 CAS latency of 5 Reserved
8-7	Reserved	0	Reserved
6-4	IBANK	0-7h 0 1h 2h 3h 4h-7h	Internal DDR2 bank setup. Defines the number of internal banks on the external DDR2 memory. 1 bank 2 banks 4 banks 8 banks Reserved
3	Reserved	0	Reserved. Always write a 0 to this bit.
2-0	PAGESIZE	0-7h 0 1h 2h 3h 4h-7h	DDR2 page size. Defines the page size of each page of the external DDR2 memory. 256-word page requiring 8 column address bits. 512-word page requiring 9 column address bits. 1024-word page requiring 10 column address bits. 2048-word page requiring 11 column address bits. Reserved

Figure 3: Configuration Table for TMS320DM644X