



## ISSI's 256Mb (8Mx32) DDR2 SDRAM Options

### INTRODUCTION

DDR2 JEDEC standard configurations for the 256Mb DDR2 SDRAM is currently limited to three data bus width options. As shown in Table 1, 256 Mb DDR2 SDRAM devices are available only in x4, x8, and x16 products. Due to the demand for x32 products, ISSI is offering a 256 Mb (8 Mb x 32) DDR2 SDRAM device.

Configuration	64 Mb x 4	32 Mb x 8	16 Mb x 16
# of banks	4	4	4
Bank Address	BA0,1	BA0,1	BA0,1
Precharge Address	A10	A10	A10
Row Address	A0-A12	A0-A12	A0-A12
Column Address	A0-A9,A11	A0-A9	A0-A8

Table 1: 256Mb DDR2 JEDEC JESD79-2E Configurations

In order to support this increased data bus width, several changes are implemented in the column and row addressing of the device. This technical note will discuss the main differences between the column and row addressing of the JEDEC Standard 256Mb DDR2 SDRAM and ISSI's 256 Mb (8 Mb x 32) DDR2 SDRAM device and the effect of these changes in system design.

### **STANDARD OPTION (IS43DR32800A) AND REDUCED PAGE-SIZE OPTION (IS43DR32801A)**

All of 256Mb DDR2 JEDEC devices have configurations that can be supported using 13 address lines (A0-A12). Due to the 8M x 32 configuration of ISSI's 256 Mb DDR2 SDRAM device, the row address width or the column address width has to be reduced by one line. In order to provide system designers flexibility in their SDRAM controller selection, ISSI's 256Mb DDR2 SDRAM device is available in two options: *Standard Page-Size* and *Reduced Page-Size*.

The Standard Page-Size option (IS43DR32800A) uses a smaller row address width but utilizes the same column address width as 256Mb DDR2 JEDEC standard devices. The Reduced Page-Size option (IS43DR32801A) has the same row address width but operates with a smaller column address width. The row and column addressing of these two options is shown in Table 2.

Option	Standard Page-Size Option (IS43DR32800A)	Reduced Page-Size Option (IS43DR32801A)
Configuration	8 Mb x 32	
# of banks	4	
Bank Address	BA0,1	BA0,1
Precharge Address	A10	A10
Row Address	<b>A0-A11</b>	<b>A0-A12</b>
Column Address	<b>A0-A8</b>	<b>A0-A7</b>
Package	126-ball BGA	126-ball BGA
Refresh	4K/64ms	8K/64ms

Table 2: ISSI's 256Mb (8M x 32) DDR2 Options

## Package Pin-Out

One of the main differences between the two options is the package pin-out. As shown in Figure 1, the Reduced-Page Size option will include an A12 pin because this option has the same row address width as the JEDEC Standard device. On the other hand, the Standard Page-Size option has one less row address line. The K4 ball will be a No Connect (NC) pin in this option.

1	2	3	4	5	6	7	8	9	10	11	12	
VDD	DQ0	VSSQ	VSS					VSS	VSSQ	DQ8	VDD	A
DQ1	VDDQ	DQ2	VDDQ					VDDQ	DQ10	VDDQ	DQ9	B
VSSQ	DQ3	VSSQ	/DQS0					/DQS1	VSSQ	DQ11	VSSQ	C
DQ4	VDDQ	DQS0	VDDQ					VDDQ	DQS1	VDDQ	DQ12	D
VSSQ	DQ5	VSSQ	DQ6					DQ14	VSSQ	DQ13	VSSQ	E
DQ7	VDDQ	DQM0	VSS					VDDQ	DQM1	VDDQ	DQ15	F
/WE	/RAS	CKE	ODT					VREF	NC/BA2	BA0	CK	G
/CAS	/CS	VDD	VDDL					VSSDL	VSSQ	BA1	/CK	H
A3	A10/AP	A1	A7					A2	A0	A6	A4	J
	A9	A5	NC/A12					NC	A11	A8		K
DQ23	VDDQ	DQM2	VSS					VDD	DQM3	VDDQ	DQ31	L
VSSQ	DQ21	VSSQ	DQ22					DQ30	VSSQ	DQ29	VSSQ	M
DQ20	VDDQ	DQS2	VDDQ					VDDQ	DQS3	VDDQ	DQ28	N
VSSQ	DQ19	VSSQ	/DQS2					/DQS3	VSSQ	DQ27	VSSQ	P
DQ17	VDDQ	DQ18	VDDQ					VDDQ	DQ26	VDDQ	DQ25	R
VDD	DQ16	VSSQ	VSS					VSS	VSSQ	DQ24	VDD	S

\* A12 for Reduced Page device IS43DR32801A

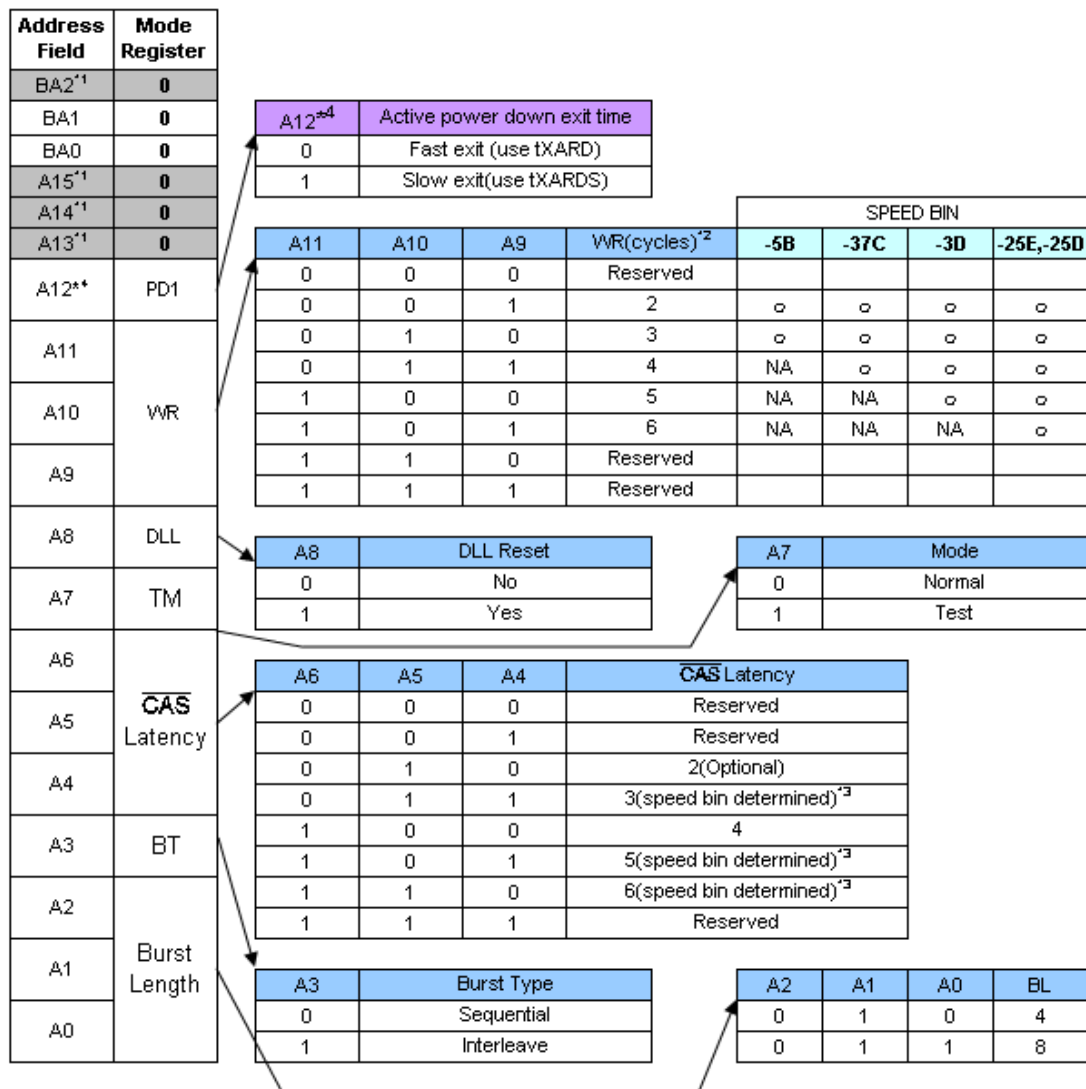
\* NC for Standard Page device IS43DR32800A

■ = Ball not populated

Ball	Name
CK, <b>CK</b>	Differential Clock Inputs
CKE	Clock Enable
<b>CS</b>	Chip Select
ODT	On Die Termination
<b>RAS</b>	Row Access Strobe
<b>CAS</b>	Column Access Strobe
<b>WE</b>	Write Enable
DM0-DM3	Input Data Mask
BA0-BA1	Bank Address Inputs
<b>A0-A12</b>	<b>Address Inputs (Reduced Page-Size)</b>
<b>A0-A11</b>	<b>Address Inputs (Standard Page-Size)</b>
DQ0-DQ31	Data I/O
DQS0-DQS3	Data Strobe
NC	No Connect
VDDQ	DQ Power Supply
VSSQ	DQ Ground
VDDL	DLL Power Supply
VSSDL	DLL Ground
VDD	Power Supply
VSS	Ground
VREF	Reference Voltage

Figure 1. 126-ball BGA package ball-out and ball list for ISSI's 256Mb (8M x 32) device

## Mode Register (MRS) and Extended Mode Register (EMRS) Setting



NOTE 1 BA2 and A13-A15 are reserved for future use and must be set to 0 when programming the MR.

NOTE 2 For DDR2-400/533, WR (write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = RU{ tWR[ns] / tCK[ns] }, where RU stands for round up). For DDR2-667/800, WR min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[ns] / tCK(avg)[ns] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

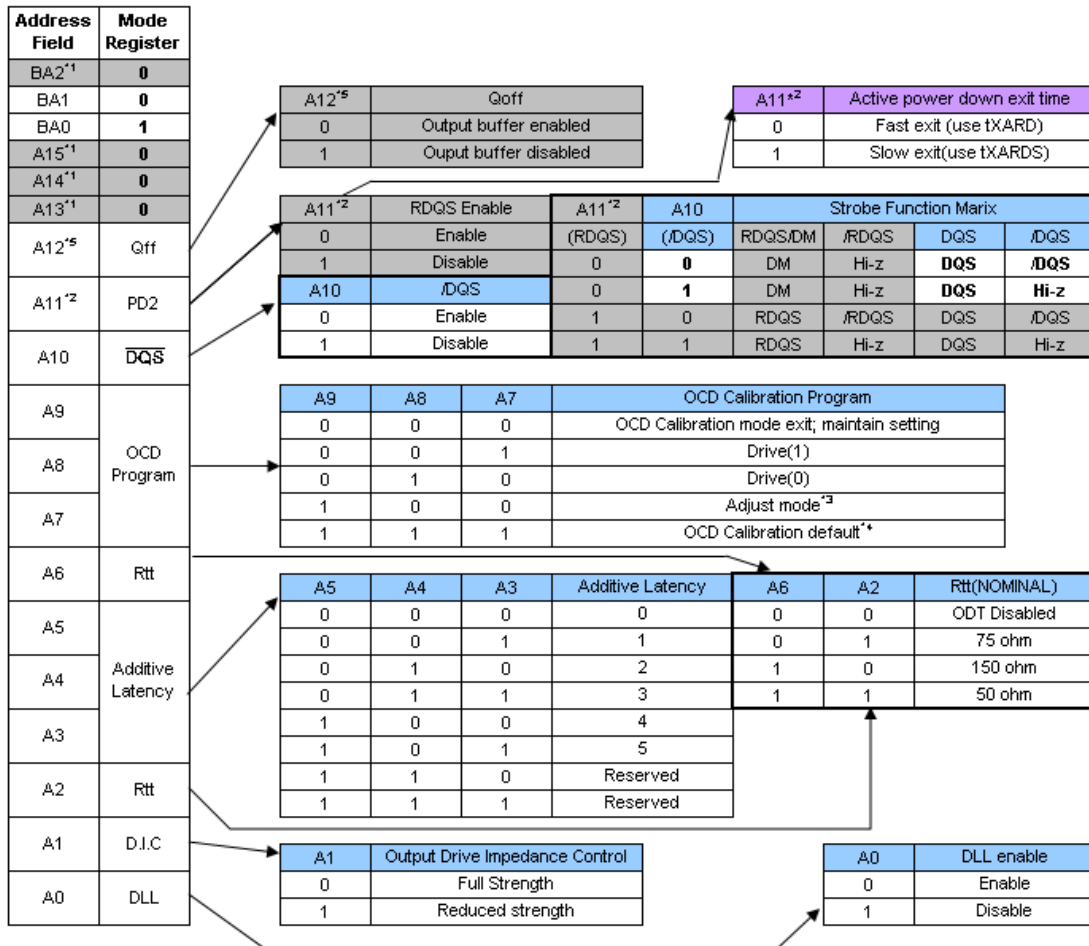
NOTE 3 Speed bin determined. Not required on all speed bins

**NOTE 4 This feature is available in MR for the Reduced Page-Size Option only. It is moved to EMR(1) A11 bit for the Standard Page-Size Option.**

Figure 2. 256Mb (8M x 32) DDR2 SDRAM Mode Register Set (MRS)

As part of the initialization process of DDR2 SDRAM devices, Mode Register Set (MRS) and Extended Mode Register Set (EMRS) commands must be issued prior to normal device operation. These commands enable user defined variables, such as burst length and CAS latency shown in Figures 2 and 3, to be programmed by controlling the state of the address pins. Any changes in the addressing of the device will affect the MRS/EMRS setting and makes the MRS/EMRS setting between the two options different.

With the A12 pin present in the reduced-page option, the mode registers in this option has the same address field assignments as the other 256Mb DDR2 JEDEC standard devices. In contrast, the Standard Page-Size option does not utilize an A12 pin. Instead, the variable assigned to the A12 address field of the mode register (MR) is reassigned to the A11 address field of the extended mode register EMR1.



NOTE 1 BA2 and A12-A15 are reserved for future use and must be set to 0 when programming the EMR(1).

**NOTE 2 x16/x32/x64 devices do not support RDQS option. Instead, it is used as the Active power down exit time for the Standard Page-Size Option.**

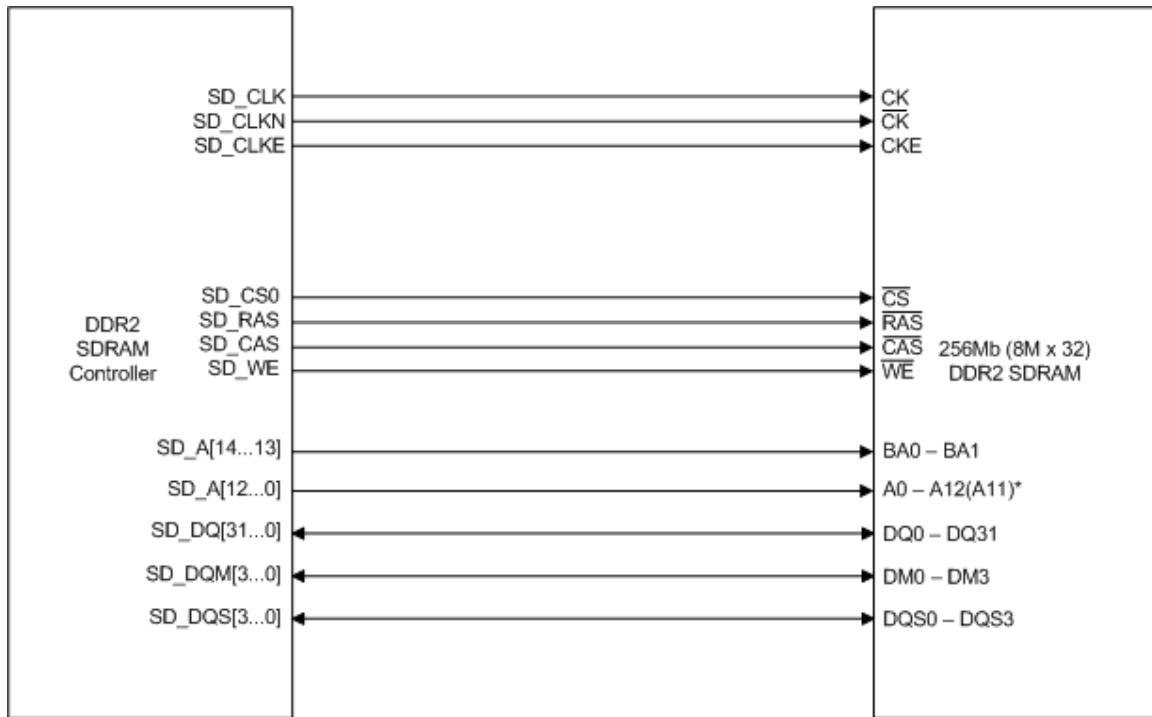
NOTE 3 When Adjust mode is issued, AL from previously set value must be applied.

NOTE 4 After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000.

NOTE 5 Output disabled - DQs, DQSs, DQSs. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included. This feature is not available in this device.

Figure 3. 256Mb (8M x 32) DDR2 SDRAM Extended Mode Register Set (EMRS) for EMR1

**SYSTEM DESIGN IMPACTS**



\*A12 is only available for the reduced page size option (IS43DR32801A)

Figure 4. System Diagram of a SDRAM controller connected to ISSI's 256Mb (8M x 32) DDR2 SDRAM

SDRAM Controllers that interface with DDR2 JEDEC Standard SDRAMs are guaranteed to support all JEDEC standard commands for x4, x8, and x16 configurations. However, ISSI's 256 Mb (8M x 32) DDR2 SDRAM device is not available as a default option. As such, programming SDRAM controllers that interface with either of the x32 device options must take note of several issues.

Normally, DDR2 SDRAM controllers program the power down exit time by setting the A12 address field of the mode register. Because the A12 address line is not available for the Standard Page-Size option, the SDRAM controller cannot set the active power down exit time setting using the standard MRS command. As shown in Figure 3, this variable must be set by the SDRAM controller using the EMRS command and enter the desired setting in the A11 address field.

Also, controllers configured to DDR2 JEDEC Standard generally support a column address width of 9 to 11 lines. However, the Reduced Page-Size Option has 8 address lines. This is a critical issue because several AC timing parameters are based on the column width of the device. In addition, assertions of certain commands, such as Precharge, also depend on the column width. Figure 5 shows how Texas Instruments' TMS320DM644x can be modified to support a DDR2 SDRAM device with 8 column address bits.

Bit	Field	Value	Description
11-9	CL	0-7h	CAS latency.
		0-1h	Reserved
		2h	CAS latency of 2
		3h	CAS latency of 3
		4h	CAS latency of 4
		5h	CAS latency of 5
		8h-7h	Reserved
8-7	Reserved	0	Reserved
6-4	IBANK	0-7h	Internal DDR2 bank setup. Defines the number of internal banks on the external DDR2 memory.
		0	1 bank
		1h	2 banks
		2h	4 banks
		3h	8 banks
4h-7h	Reserved		
3	Reserved	0	Reserved. Always write a 0 to this bit.
2-0	PAGESIZE	0-7h	DDR2 page size. Defines the page size of each page of the external DDR2 memory.
		0	256-word page requiring 8 column address bits.
		1h	512-word page requiring 9 column address bits.
		2h	1024-word page requiring 10 column address bits.
		3h	2048-word page requiring 11 column address bits.
4h-7h	Reserved		

Figure 5. Texas Instruments' TMS320DM644x SDRAM Bank Configuration

## CONCLUSION

Due to the difference in their page size and addressing, each option has its advantages and disadvantages. The Standard Page-Size Option (IS43DR32800A) allows the use of 9 column address lines. However, the SDRAM controller has to set the mode registers differently due to the lack of an A12 pin. The Reduced Page-Size option (IS43DR32801A) allows the use of the A12 pin for normal setting of both the mode and extended mode registers. As a result, the designer has to use a lower column address width of 8 lines.

Figure 6 shows a flowchart to help system engineers choose which part is more suited for their design. If their design will incorporate an SDRAM controller that will allow them to modify the column address size to support a 256 word page size using 8 address lines, the best option is the Reduced Page-Size Option (IS43DR801A) because this device is MRS/EMRS JEDEC compliant. This allows them to initialize the mode registers using the same process as other DDR2 JEDEC Standard devices. If the design requires at least 9 column address lines, the Standard Page-Size Option (IS43DR800A) is the correct choice.

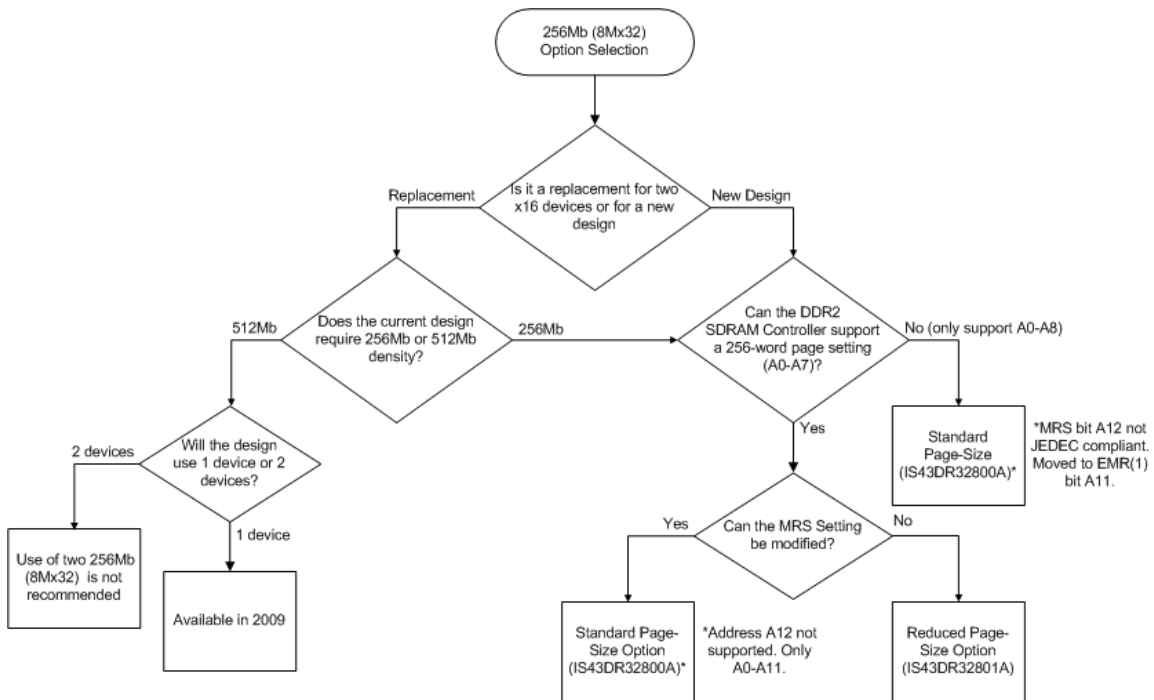


Figure 6. Option Selection Flowchart

## References

- [1] DDR2 SDRAM Specification, JEDEC JESD79-2E, April 2008.
- [2] IS43DR800A/IS43DR801A Datasheet
- [3] TMS320DM644x DMSoC DDR2 Memory Controller User's Guide, November 2007