Table 38. CFI Primary Vendor-Specific Extended Query (Continued)

Word Address	Data	Description
(SA) + 0050h	0001h	Program Suspend 00 = Not Supported 01 = Supported
(SA) +0051h	0000h	Unlock Bypass 00 = Not Supported 01 = Supported
(SA) + 0052h	000Ah	Secure Silicon Sector (Customer OTP Area = 1024B) Size 2^N (bytes)
(SA) + 0053h	008Dh	Software Features Bit 0: Status Register polling (1 = Supported, 0 = Not Supported) Bit 1: DQ polling (1 = Supported, 0 = Not Supported) Bit 2: New Program Suspend / Resume commands (1 = Supported, 0 = Not Supported) Bit 3: Word Programming (1 = Supported, 0 = Not Supported) Bit 4: Bit-Field Programming (1 = Supported, 0 = Not Supported) Bit 5: Autodetect Programming (1 = Supported, 0 = Not Supported) Bit 6: RFU Bit 7: Multiple Writes per Line (1 = Supported, 0 = Not Supported)
(SA) + 0054h	0005h	Page Size = 2^N bytes
(SA) + 0055h	0006h	Erase Suspend Timeout Maximum < 2^N (µs)
(SA) + 0056h	0006h	Program Suspend Timeout Maximum < 2^N (µs)
(SA) + 0057h to (SA) + 0077h	FFFFh	Reserved for Future Use
(SA) + 0078h	0006h	Embedded Hardware Reset Timeout Maximum < 2^N (µs) Reset with Reset Pin
(SA) + 0079h	0009h	Non-Embedded Hardware Reset Timeout Maximum < 2^N (µs) Power-On Reset

7.2 Device ID and Common Flash Interface (ID-CFI) ASO Map — Automotive Grade / AEC-Q100

The CFI Primary Vendor-Specific Extended Query for Automotive Grade / AEC-Q100 is extended to include Electronic Marking information for device traceability (see Table 39).

Table 39. Device ID and Common Flash Interface (ID-CFI) ASO Map (1)

Word Address	Data Field	Number of Bytes	Data Format	Example of Actual of Data	Hex Read Out of Example Data
(SA) + 0080h	Size of Electronic Marking	1	Hex	19	0013h
(SA) + 0081h	Revision of Electronic Marking	1	Hex	1	0001h
(SA) + 0082h	Fab Lot #	7	ASCII	LD87270	004Ch, 0044h, 0038h, 0037h, 0032h, 0037h, 0030h
(SA) + 0089h	Wafer #	1	Hex	23	0017h
(SA) + 008Ah	Die X Coordinate	1	Hex	10	000Ah
(SA) + 008Bh	Die Y Coordinate	1	Hex	15	000Fh
(SA) + 008Ch	Class Lot #	7	ASCII	BR33150	0042h, 0052h, 0033h, 0033h, 0031h, 0035h, 0030h
(SA) + 0093h	Reserved for Future	13	NA	NA	Undefined

Note:
1. Fab Lot # + Wafer # + Die X Coordinate + Die Y Coordinate provides unique ID for each device.

8. Software Interface Reference

8.1 Command Summary

Table 40. Command Definitions

Command Sequence	Cycles	Bus Cycles (Notes 1 - 4)													
		First		Second		Third		Fourth		Fifth		Sixth		Seventh	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)	1	RA	RD												
Reset / ASO Exit (6), (14)	1	XXX	F0												
Status Register Read (16)	2	555	70	XXX	RD										
Status Register Clear	1	555	71												
Enter Deep Power-Down	3	555	AA	2AA	55	XXX	B9								
Program Power-On Reset Timer Register	4	555	AA	2AA	55	555	34	XXX	PORTime						
Read Power-On Reset Timer Register	4	555	AA	2AA	55	555	3C	XXX	RD PORTime						
Load Interrupt Configuration Register	4	555	AA	2AA	55	555	36	XXX	ICR						
Read Interrupt Configuration Register	4	555	AA	2AA	55	555	C4	XXX	RD ICR						
Load Interrupt Status Register	4	555	AA	2AA	55	555	37	XXX	ISR						
Read Interrupt Status Register	4	555	AA	2AA	55	555	C5	XXX	RD ISR						
Load Volatile Configuration Register	4	555	AA	2AA	55	555	38	XXX	VCR						
Read Volatile Configuration Register	4	555	AA	2AA	55	555	C7	XXX	RD VCR						
Program Non-Volatile Configuration Register	4	555	AA	2AA	55	555	39	XXX	NVCR						
Erase Non-Volatile Configuration Register	3	555	AA	2AA	55	555	C8								
Read Non-Volatile Configuration Register	4	555	AA	2AA	55	555	C6	XXX	RD NVCR						
Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
Program Buffer to Flash (confirm)	1	SA	29												
Write-to-Buffer-Abort Reset (10)	3	555	AA	2AA	55	555	F0								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Blank Check	1	(SA) 555	33												
Evaluate Erase Status	1	(SA) 555	D0												
Erase Suspend	1	XXX	B0												
Erase Resume	1	XXX	30												
Program Suspend	1	XXX	51												
Program Resume	1	XXX	50												

Table 40. Command Definitions (Continued)

Command Sequence		Cycles	Bus Cycles (Notes 1 - 4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
ID-CFI (Autoselect) ASO (19)	ID (Autoselect) Entry	3	555	AA	2AA	55	(SA) 555	90								
	CFI Enter (Note 7)	1	(SA) 555	98												
	ID-CFI Read	1	(SA) RA	RD												
	Reset / ASO Exit (6), (14)	1	XXX	F0 or FF												
Secure Silicon Region Command Definitions																
Secure Silicon Region (SSR) ASO	SSR Entry	3	555	AA	2AA	55	(SA) 555	88								
	Read (5)	1	RA	RD												
	Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
	Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
	Program Buffer to Flash (confirm)	1	SA	29												
	Write-to-Buffer-Abort Reset (10)	3	555	AA	2AA	55	555	F0								
	SSR Exit (10)	4	555	AA	2AA	55	555	90	XX	00h						
	Reset / ASO Exit (6), (14)	1	XXX	F0												
ASP Config. Register (ASPR) ASO	ASP Register Entry	3	555	AA	2AA	55	555	40								
	Program	2	XXX	A0	XXX	PD										
	ASPR Read (16)	1	0	RD												
	ASPR ASO Exit (10)	2	XXX	90	XXX	0										
	Reset / ASO Exit (6), (14)	1	XXX	F0												
Password Protection Command Set Definitions																
Password ASO	Password ASO Entry	3	555	AA	2AA	55	555	60								
	Program (12)	2	XXX	A0	PWA x	PWDx										
	Read	4	0	PWD 0	1	PWD 1	2	PWD 2	3	PWD 3						
	Unlock	7	0	25	0	3		PWD 0	1	PWD 1	2	PWD 2	3	PWD 3	0	29
	Command Set Exit (11), (14)	2	XXX	90	XXX	0										
	Reset / ASO Exit (6), (14)	1	XXX	F0												

Table 40. Command Definitions (Continued)

	Command Sequence	Cycles	Bus Cycles (Notes 1 - 4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Non-Volatile Sector Protection Command Set Definitions																
PPB (Non-Volatile Sector Protection)	PPB Entry	3	555	AA	2AA	55	555	C0								
	PPB Program (15)	2	XXX	A0	SA	0										
	All PPB Erase (15)	2	XXX	80	0	30										
	PPB Read (15), (16)	1	SA	RD (0)												
	SA Protection Status (16), (17)	2	XXX	60	SA	RD										
	Command Set Exit (11), (14)	2	XXX	90	XXX	0										
	Reset / ASO Exit (6), (14)	1	XXX	F0												
Global Non-Volatile Sector Protection Freeze Command Set Definitions																
PPB Lock Bit	PPB Lock Entry	3	555	AA	2AA	55	555	50								
	PPB Lock Bit Clear	2	XXX	A0	XXX	0										
	PPB Lock Status Read (16)	1	XXX	RD (0)												
	Command Set Exit (11), (14)	2	XXX	90	XXX	0										
	Reset / ASO Exit (14)	1	XXX	F0												
Volatile Sector Protection Command Set Definitions																
DYB (Volatile Sector Protection) ASO	DYB ASO Entry	3	555	AA	2AA	55	555	E0								
	DYB Set (15)	2	XXX	A0	SA	0										
	DYB Clear (15)	2	XXX	A0	SA	1										
	DYB Status Read (16)	1	SA	RD (0)												
	SA Protection Status (15), (16), (17)	2	XXX	60	SA	RD										
	Command Set Exit (11), (14)	2	XXX	90	XXX	0										
	Reset / ASO Exit (14)	1	XXX	F0												
ECC Command Set Definitions																
ECC Status ASO	ECC Status Enter	3	555	AA	2AA	55	555	75								
	ECC Status Read (16)	1	RA	RD												
	Error Lower Address Register	2	XXX	60	xx1	RD										
	Error Upper Address Register	2	XXX	60	xx2	RD										
	Read Error Detection Counter	2	XXX	60	xx3	RD										
	Clear ECC Errors	1	XXX	50												
	Reset/ASO Exit	1	XXX	F0												
CRC Command Set Definitions																

Table 40. Command Definitions (Continued)

Command Sequence		Cycles	Bus Cycles (Notes 1 - 4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
CRC ASO	CRC ASO Entry	3	555	AA	2AA	55	555	78								
	Load CRC Start Address	1	BL	C3												
	Load CRC End Address (start calculation)	1	EL	3C												
	CRC Suspend	1	XXX	C0												
	Array Read (during suspend)	1	RA	RD												
	CRC Resume	1	XXX	C1												
	Read Check-value Low Result Register	2	XXX	60	XX0	RD										
	Read Check-value High Result Register	2	XXX	60	XX1	RD										
	Reset / ASO Exit	1	XXX	F0												

Command Definitions Legend:
X = Don't care.
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed.
PD = Data to be programmed at location PA.
SA = Address of the sector selected. Address bits A_{MAX}-A17 for 256-kB sectors and A_{MAX}-A11 for 4-kB parameter sectors uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same Line.
WC = Word Count is the number of write buffer locations to load minus 1.
PWAx = Password address for word0 = 00h, word1 = 01h, word2 = 02h, and word3 = 03h.
PWDx = Password data word0, word1, word2, and word3.

Notes:
1. *All values are in hexadecimal. All addresses reference 16-bit words.*
2. *Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.*
3. *Data bits DQ15-DQ8 are 'don't care' in command sequences, except for RD, PD, WC and PWD.*
4. *Address bits A_{MAX}-A11 are 'don't care' for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.)*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the ID-CFI (Autoselect) Mode, or if DQ5 goes High (while the device is providing status data).*
7. *Command is valid when device is ready to read array data or when device is in ID-CFI (Autoselect) Mode.*
8. *The system can read and program / program suspend in non-erasing sectors, or enter the ID-CFI ASO, when in the Erase Suspend Mode. The Erase Suspend command is valid only during a sector erase operation.*
9. *The Erase Resume / Program Resume command is valid only during the Erase Suspend / Program Suspend Modes.*
10. *Issue this command sequence to return to READ Mode after detecting device is in a Write-to-Buffer-Abort state. Note that the full command sequence is required if resetting out of ABORT.*
11. *The Exit command returns the device to reading the array.*
12. *For PWDx, only one portion of the password can be programmed per each 'A0' command. Portions of the password must be programmed in sequential order (PWD0-PWD3).*
13. *All ASP Register bits are one-time programmable. The program state = 0 and the erase state = 1. Both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the ASPR Register Bits Program operation aborts and returns the device to Read Mode. ASPR Register bits that are reserved for future use are undefined and may be 0's or 1's.*
14. *If any of the Entry commands was issued, an Exit command must be issued to reset the device into Read Mode.*
15. *Bit 0 = 0 indicates the Protected State, Bit 0 = 1 indicates the Unprotected State. Bits 1 through 15 are all 1s. The sector address for DYB set, DYB clear, or PPB Program command may be any location within the sector; the lower order bits of the sector address are 'don't care'.*
16. *Data out during a Status Register Read transaction, DYB Read, PPB Read, SA Protection Read, Password Read, POR Timer Read, ICR Read, ISR Read, VCR Read, NVCR Read, FIDR Read, ASPR Read, PPBL Read Register Read transactions is only valid during the first word output by the device. Subsequent data values output if CK/CK# continue to toggle while CS# remains Low are undefined.*

17. *Data out during a SA Protection Status Read indicates whether the indicated sector is protected in bits 0-2.*
    Bit 0 – Indicates whether the indicated sector is protected (0 = protected, 1 = unprotected).
    Bit 1 – Protected using the sector's DYB bit (0 = protected, 1 = unprotected).
    Bit 2 – Protected using the sector's PPB bit (0 = protected, 1 = unprotected).
    Bits 3 through 15 are all 1s.
18. *The smaller parameter-sectors need to include A[16:11] as part of the address identifying the target parameter-sector during erase and program command sequences.*
19. *Both the ID (Autoselect) Entry and the CFI Entry allows access to the same ID/CFI data set. All data contained in within the ID/CFI data set is available after using either the ID or CFI Entry sequences.*

9. Data Integrity

9.1 Endurance

Program / Erase Endurance

Non-Volatile Unit	Temperature Range	Minimum	Unit
Any Sector	Industrial	100K	Program-Erase cycles
	Industrial Plus	100K	
	Extended	10K	
Configuration Register	Industrial	100K	
	Industrial Plus	100K	
	Extended	10K	

Note:
1. Cycling data collection was limited to 100K cycles.

9.2 Data Retention

Data Retention

Parameter	Typical	Unit
Data Retention Time after 1K cycles or less with one programming operation, per half-page, per erase	20	Years

Hardware Interface

For the general description of the HyperBus hardware interface of HyperFlash memories refer to the HyperBus Specification. The following section describes HyperFlash device dependent aspects of hardware interface.

10. Electrical Specifications

The following section describes HyperFlash device dependent aspects of electrical specifications.

10.1 Absolute Maximum Ratings

Storage Temperature Plastic Packages-	65 °C to +150 °C
Ambient Temperature with Power Applied	–65 °C to +125 °C
Voltage with Respect to Ground	
All signals (1)	–0.5 V to +(V_{CC} + 0.5 V)
Output Short Circuit Current (2)	100 mA
V_{CC}	–0.5 V to +4.0 V

Notes:

1. *Minimum DC voltage on input or I/O signal is -1.0 V. During voltage transitions, input or I/O signals may undershoot V_{SS} to -1.0 V for periods of up to 20 ns. See Figure 20. Maximum DC voltage on input or I/O signals is V_{CC} +1.0 V. During voltage transitions, input or I/O signals may overshoot to V_{CC} +1.0 V for periods up to 20 ns. See Figure 21.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

10.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{DD}. During voltage transitions, inputs or I/Os may negative overshoot V_{SS} to -1.0V or positive overshoot to V_{DD} +1.0V, for periods up to 20 ns.

Figure 20. Maximum Negative Overshoot Waveform

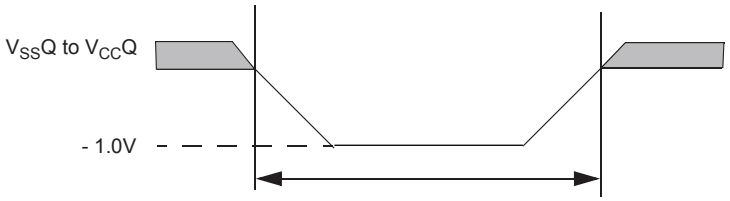
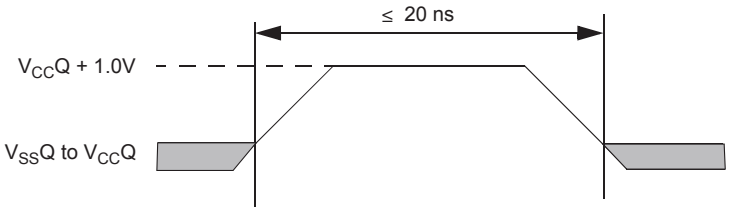


Figure 21. Maximum Positive Overshoot Waveform



10.2 Thermal Impedance

Parameter	Description	VAA024	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	43.5	°C/W

Note:
1. Test conditions follow standard methods and procedures for measuring thermal impedance in accordance with EIA/JESD51.

10.3 Latchup Characteristics

Table 41. Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to $V_{SS}Q$ on all input only connections	–1.0	V_{CCQ} + 1.0	V
Input voltage with respect to $V_{SS}Q$ on all I/O connections	–1.0	V_{CCQ} + 1.0	V
$V_{CC}Q$ Current	–100	+100	mA

Note:
1. Excludes power supplies V_{CC}/V_{CCQ}. Test conditions: $V_{CC} = V_{CCQ} = 1.8$ V, one connection at a time tested, connections not being tested are at V_{SS}.

10.4 Operating Ranges

Operating ranges define those limits between which the functionality of a device is guaranteed. The operating range is device specific. Consult the device data sheet Ordering Part Number valid combinations to know which operating ranges are supported by a particular device.

10.4.1 Temperature Ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial	–40	+85	°C
		Extended	–40	+105	
		Extended+	–40	+125	
		Automotive, AEC-Q100 Grade A1	–40	+85	
		Automotive, AEC-Q100 Grade A2	–40	+105	
		Automotive, AEC-Q100 Grade A3	–40	+125	

10.4.2 Power Supply Voltages

V_{CC} and $V_{CC}Q$	1.7V to 1.95V
V_{CC} and $V_{CC}Q$	2.7V to 3.6V

10.5 DC Characteristics (CMOS Compatible)

Table 42. DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions	Min	Typ (9)	Max	Unit
I_{CC1}	V_{CC} Active Read Current (core current only, IO switching current is not included)	CS# = V_{IL}, @166 MHz, V_{CC} = 1.95V		130	180	mA
		CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V		80	100	mA
I_{IO1}	$V_{CC}Q$ Active Read Current of IOs	CS# = V_{IL}, @166 MHz, $V_{CC}Q$ = 1.95V, C_{LOAD} = 20 pf		80	100	mA
		CS# = V_{IL}, @100 MHz, $V_{CC}Q$ = 3.6V, C_{LOAD} = 20 pf		80	100	mA
I_{CC3P}	V_{CC} Active Program Current (1), (2)	V_{CC} = V_{CC} max		60	100	mA
I_{CC3E}	V_{CC} Active Erase Current (1), (2)	V_{CC} = V_{CC} max		60	100	mA
I_{CC4I}	V_{CC} Standby Current for Industrial Temp. (–40°C to +85°C)	CS# = V_{IH}, RESET# = V_{CC}, V_{CC} = V_{CC} max		25	100	µA
I_{CC4IC}	V_{CC} Standby Current for Industrial Plus (Automotive - In Cabin) Temp. (–40°C to +105°C)	CS# = V_{IH}, RESET# = V_{CC}, V_{CC} = V_{CC} max		25	300	µA
I_{CC4E}	V_{CC} Standby Current for Extended Temp. (–40°C to +125°C)	CS# = V_{IH}, RESET# = V_{CC}, V_{CC} = V_{CC} max		25	300	µA
I_{CC5}	V_{CC} Reset Current (5)	CS# = V_{IH}, RESET# = V_{SS}, V_{CC} = V_{CC} max		10	20	mA
I_{CC6}	Active Clock Stop Mode (3)	V_{IH}= V_{CC}, V_{IL} = V_{SS}, V_{CC} = 1.95V		6	12	mA
		V_{IH}= V_{CC}, V_{IL} = V_{SS}, V_{CC} = 3.6V		6	12	mA
I_{CC7}	V_{CC} Current during Power-Up (4)	CS# = X, V_{CC} = V_{CC} max,		80	100	mA
I_{DPD}	Deep Power-Down Current 512 Mb @ 25 °C	CS# = V_{IH}, RESET#, V_{CC} = V_{CC} max		8	18	µA
	Deep Power-Down Current 512 Mb @ 85 °C			30	50	µA
	Deep Power-Down Current 512 Mb @ 105 °C			95	150	µA
	Deep Power-Down Current 512 Mb @ 125 °C			150	250	µA
	Deep Power-Down Current (all other densities) @ 25 °C			3	6	µA
	Deep Power-Down Current (all other densities) @ 85 °C			4	10	µA
	Deep Power-Down Current (all other densities) @ 105 °C			5	15	µA
	Deep Power-Down Current 256 Mb @ 125 °C			15	25	µA
	Deep Power-Down Current 128 Mb @ 125 °C			10	15	µA
V_{IL}	Input Low Voltage		-0.15 x $V_{CC}Q$	–	0.35 x $V_{CC}Q$	V

Notes:

1. *I_{CC} active while Embedded Algorithm is in progress.*
2. *Not 100% tested.*
3. *Active Clock Stop Mode enables the lower power mode when the CK/CK# signals remain stable for t_{ACC} + 30 ns.*
4. *$V_{CC}Q$ = 1.70V to 1.95V or 2.7V to 3.6V.*
5. *V_{CC} = $V_{CC}Q$ = 1.8V or V_{CC} = $V_{CC}Q$ = 3.0V.*
6. *During Power-Up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.*
7. *If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to Standby Mode until the next read or write.*
8. *The recommended pull-up resistor for the INT# and RSTO# outputs is 5k to 10k Ohms.*
9. *Typical I_{CC} values are measured at t_{AI} = 25°C and V_{CC} = $V_{CC}Q$ = 1.8V or 3.0V (not applicable to I_{DPD} for 85°C and 105°C).*

Table 42. DC Characteristics (CMOS Compatible) continued

Parameter	Description	Test Conditions	Min	Typ (9)	Max	Unit
V_{IH}	Input High Voltage		0.65 x $V_{CC}Q$	–	1.15 x $V_{CC}Q$	V
V_{OH}	Output High Voltage	I_{OH} = 100 µA for DQ[7:0]	$V_{CC}Q$ - 0.20	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA for DQ7-DQ0 I_{OL} = 2 mA for INT# and RSTO#	–	–	0.15 x $V_{CC}Q$	V

Notes:

1. *I_{CC} active while Embedded Algorithm is in progress.*
2. *Not 100% tested.*
3. *Active Clock Stop Mode enables the lower power mode when the CK/CK# signals remain stable for t_{ACC} + 30 ns.*
4. *$V_{CC}Q$ = 1.70V to 1.95V or 2.7V to 3.6V.*
5. *V_{CC} = $V_{CC}Q$ = 1.8V or V_{CC} = $V_{CC}Q$ = 3.0V.*
6. *During Power-Up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.*
7. *If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to Standby Mode until the next read or write.*
8. *The recommended pull-up resistor for the INT# and RSTO# outputs is 5k to 10k Ohms.*
9. *Typical I_{CC} values are measured at t_{AI} = 25°C and V_{CC} = $V_{CC}Q$ = 1.8V or 3.0V (not applicable to I_{DPD} for 85°C and 105°C).*

10.5.1 Capacitance Characteristics

Table 43. 1.8V Capacitive Characteristics

Description	Parameter	Min	Max	Unit
Input Capacitance (CK, CK#, CS#, PSC, PSC#)	CI	3.5	4.5	pF
Delta Input Capacitance (CK, CK#, CS#, PSC, PSC#)	CID	—	0.25	pF
Output Capacitance (RWDS)	CO	5.0	6.0	pF
I/O Pin Capacitance (DQx)	CIO	5.0	6.0	pF
I/O Pin Capacitance Delta (DQx)	CIOD	—	0.8	pF
INT#, RSTO# Pin Capacitance	COP	5.0	6.0	pF
WP#, RESET# Pin Capacitance	CIP	6.5	9.0	pF

Notes:

1. *These values are guaranteed by design and are tested on a sample basis only.*
2. *Pin capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, $V_{CC}Q$ are applied and all other pins (except the pin under test) floating. DQs should be in the High Impedance state.*
3. *The capacitance values for the CK, CK#, RWDS and DQx pins must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.*

Table 44. 3.0V Capacitive Characteristics

Description	Parameter	Min	Max	Unit
Input Capacitance (CK, CS#)	CI	3.5	4.5	pF
PSC	CI	3.5	4.5	pF
Output Capacitance (RWDS)	CO	4.5	6.0	pF
I/O Pin Capacitance (DQx)	CIO	4.5	6.0	pF
I/O Pin Capacitance Delta (DQx)	CIOD	—	0.8	pF
INT#, RSTO# Pin Capacitance	COP	5.0	6.0	pF
RESET# Pin Capacitance	CIP	6.0	8.5	pF

Notes:

1. *These values are guaranteed by design and are tested on a sample basis only.*
2. *Pin capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, $V_{CC}Q$ are applied and all other pins (except the pin under test) floating. DQs should be in the High Impedance state.*
3. *The capacitance values for the CK, RWDS and DQx pins must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.*

10.6 Power-Up and Power-Down

The memory is considered to be powered-off when the core power supply (V_{CC}) drops below the V_{CC} lock-out voltage (V_{LKO}). When V_{CC} is below V_{LKO}, the entire memory array is protected against a program or erase operation. This ensures that no spurious alteration of the memory content can occur during power transition. During a power supply transition down to the V_{SS} level, $V_{CC}Q$ should remain less than or equal to V_{CC}.

If V_{CC} goes below V_{CC} Reset (V_{RST}) then returns above V_{RST} to V_{CC} minimum, the Power-On Reset interface state is entered and the EAC starts the Cold Reset Embedded Algorithm.

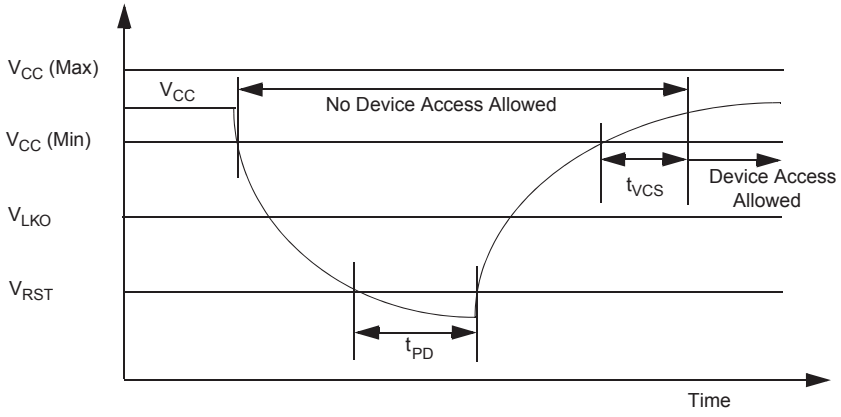
V_{CC} must always be greater than or equal to $V_{CC}Q$ ($V_{CC} \geq V_{CC}Q$).

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and $V_{CC}Q$ both rise above, and stay above, the minimum V_{CC} thresholds. During t_{VCS} the device is performing Power-On Reset operations.

During Power-Down or voltage drops below V_{LKO}, the V_{CC} voltages must drop below V_{RST} for a period of t_{PD} for the part to initialize correctly when V_{CC} and $V_{CC}Q$ again rise to their operating ranges. See Figure 22. If during a voltage drop the V_{CC} stays above V_{LKO} the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If the part locks up from improper initialization, a Software Reset can be used to initialize the part correctly.

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and $V_{CC}Q$ power supplies. Each device in a system should have the V_{CC} and $V_{CC}Q$ power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 µF).

Figure 22. Power-Down or Voltage Drop



Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	1.7	1.95	V
V_{LKO}	V_{CC} Cut-0ff below which re-initialization is required	1.5	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.5	–	V
t_{VCS}	V_{CC} and $V_{CC}Q \geq$ minimum to first access RESET# Low to High transition to first access (V_{CC} and $V_{CC}Q \geq$ minimum)	–	300	µs
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	10	–	µs

Note:
1. V_{CC} ramp rate can be non-linear.

Table 46. 3.0V Power-Up / Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	2.7	3.6	V
V_{LKO}	V_{CC} Cut-0ff below which re-initialization is required	2.4	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.7	–	V
t_{VCS}	V_{CC} and $V_{CC}Q \geq$ minimum to first access RESET# Low to High transition to first access (V_{CC} and $V_{CC}Q \geq$ minimum)	–	300	µs
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	10	–	µs

Note:
1. V_{CC} ramp rate can be non-linear.

10.6.1 Power-On (Cold) Reset (POR)

When power is first applied, with supply voltage below V_{LKO} then rising to reach operating range minimum, internal device configuration and Cold Reset activities are initiated. RESET# and CS# are ignored during the duration of the POR operation (t_{VCS}) and any user extended period of RSTO# LOW. Command sequences are blocked while the device is in the POR state or RSTO# is LOW. During this period, the device can not be selected, will not accept commands, and does not drive outputs other than RSTO#. RESET# LOW during this POR period is optional. If RESET# is driven LOW during POR it must satisfy the Hardware Reset parameters t_{RP} and t_{RPH} in which case the POR operations will be completed at the end of t_{VCS} and t_{RPH}. If RESET# is LOW during t_{VCS} it may remain LOW at the end of t_{VCS} to hold the device in the Hardware Reset state. If RESET# is HIGH at the end of t_{VCS} the device will go to the Standby state. CS# must go to V_{IH} before the end of RSTO# LOW.

During Cold Reset the device will draw I_{CC7} current. If CS# is Low during t_{VCS} the device may draw higher than typical POR current during t_{VCS} but will not exceed the maximum, and the level of CS# will not affect the Cold Reset EA.

If POR has not been properly completed by the end of t_{VCS}, a later transition to the Hardware Reset state will cause a transition to the Power-On Reset interface state and initiate the Cold Reset Embedded Algorithm. This ensures the device can complete a Cold Reset even if some aspect of the system Power-On voltage ramp-up causes the POR to not initiate or complete correctly.

RSTO# is an open-drain output used to indicate when a POR is occurring within the device and can be used as a system level reset signal. Upon completion of the internal POR the RSTO# signal will transition from Low to high impedance after a user defined timeout period has elapsed. Upon transition to the high impedance state the external pull-up resistance will pull RSTO# High and the device immediately is placed into the Standby state. While RSTO# is low, no commands are accepted by the device.

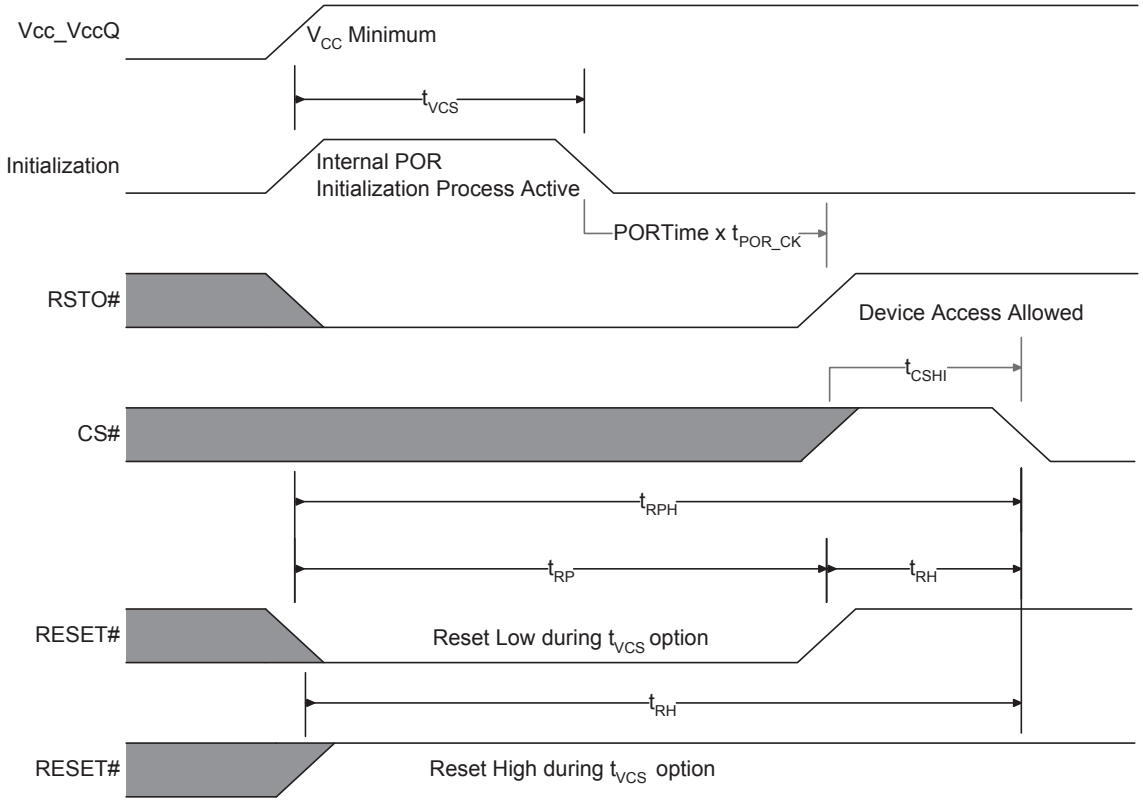
If the user wants to extend the RSTO# period beyond the POR (t_{VCS}) period the non-volatile PORTime Register must be programmed. The default value for this register (FFFFh), provides zero added time. The RSTO# signal will return to high impedance at the end of t_{VCS}. A value programmed into the 16-bit PORTime Register is multiplied by t_{POR_CK} (see Table 47. User POR Extension Clock Timings) to define the length of extension to the RSTO# pulse beyond t_{VCS}. The length of the programmed extension to the RSTO# assertion is the value programmed into the PORTime Register plus one clock cycle. The PORTime Register is OTP and, once programmed, will fail subsequent programming attempts.

Table 47. User POR Extension Clock Timings

Parameter	Symbol	Min	Max	Unit
POR Extension Clock Period	t_{POR_CK}	25	42	µs

Note that both the RSTO# and INT# outputs are undefined while V_{CC} is below V_{CC}(min). By the time that V_{CC}(min) is reached, the INT# output will be in the high impedance state. The RSTO# output will transition from the Low to high impedance state after t_{VCS}, plus any additional user defined POR extension time, after V_{CC}(min) has been reached.

Figure 23. Power On Reset Signal Diagram



Notes:

1. $V_{CC}Q$ must be the same voltage as V_{CC}.
2. PORTime is a customer programmed configuration register intended to allow RSTO# assertion beyond t_{VCS}. PORTime is described in Table 14. Non-Volatile Configuration Registers.
3. t_{POR_CK} is the internal (on-chip) clock period used to generate the extension to RSTO#. t_{POR_CK} is described in Table 47. User POR Extension Clock Timings.

10.6.2 Hardware Reset

- Terminates any operation in progress
- DQ[7:0] are placed into the High-Z state when RESET# is Low
- Exits any ASO
- Tristates all outputs
- Resets the Status Register
- Resets the EAC to Standby state
- CS# is ignored for the duration of the reset operation (t_{RPH})
- To meet the Reset current specification (I_{CC5}) CS# must be held High

To ensure data integrity any non-volatile operation that was interrupted should be reinitiated once the device completes the Hardware Reset process.

10.6.3 Hardware (Warm) Reset

The RESET# input provides a hardware method of resetting the device to the Standby state. While RESET# is Low command sequences and read operations are not allowed. Command sequences are blocked while the device is in the reset state.

During Hardware Reset the device will draw I_{CC5} current. When RESET# continues to be held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater.

A Hardware Reset will cause the bus configuration to be defined by the Non-Volatile Configuration Register (NVCR). See Figure 24. Hardware Reset Timing Diagram.

After the device has completed POR and entered the Standby state, any later transition to the Hardware Reset state will initiate the Warm Reset Embedded Algorithm. A Warm Reset is much shorter than a Cold Reset, taking tens of µs (t_{RPH}) to complete. During the Warm Reset EA, any in progress Embedded Algorithm is stopped and the EAC is returned to its POR state without reloading EAC algorithms from non-volatile memory. After the Warm Reset EA is completed, the interface will remain in the Hardware Reset state if RESET# remains Low. When RESET# returns High the interface will transition to the Standby state. If RESET# is High at the end of the Warm Reset EA, the interface will directly transition to the Standby state.

If POR has not been properly completed by the end of t_{VCS}, a later transition to the Hardware Reset state will cause a transition to the Power-On Reset interface state and initiate the Cold Reset Embedded Algorithm. This ensures the device can complete a Cold Reset even if some aspect of the system Power-On voltage ramp-up causes the POR to not initiate or complete correctly.

Figure 24. Hardware Reset Timing Diagram

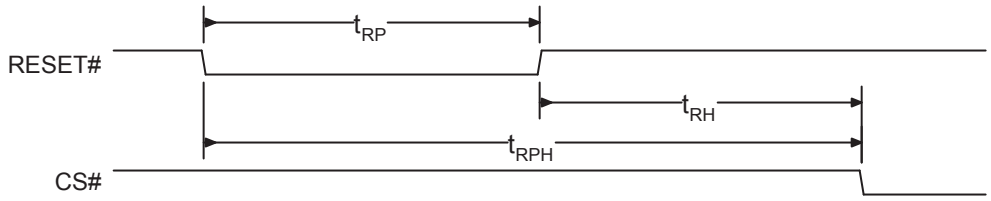


Table 48. Power-On and Reset Parameters

Parameter	Description	Limit	Time	Unit
t_{VCS}	V_{CC} Setup Time to first access[1]	Min	300	µs
t_{RPH}	RESET# Low to CS# Low	Min	30	µs
t_{RP}	RESET# Pulse Width	Min	200	ns
t_{RH}	Time between RESET# (High) and CS# (Low)	Min	150	ns
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	Min	1	µs
t_{CSHI}	Chip Select High Between Operations	Min	6.0	ns

Notes:

1. *Bus transactions (read and write) are not allowed during the Power-Up Reset time (t_{VCS}).*
2. *Timing measured from V_{CC} reaching V_{CC} min to V_{IH} on Reset and V_{IL} on CS#.*
3. *RESET# Low is optional during POR. If RESET is asserted during POR, the later of t_{RPH} and t_{VCS} will determine when CS# may go Low. If RESET# remains Low after t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VCS}. RESET must also be High t_{RH} before CS# goes Low.*
4. *V_{CC} ramp rate can be non-linear.*
5. *Sum of t_{RP} + t_{RH} must be equal to or greater than t_{RPH}.*

Hardware Reset can also be used to exit from DPD mode. Driving the RESET# input Low (for the minimum t_{RP} time) will also cause the device to exit the DPD Mode. The device will take t_{DPDOUT} to return to the Standby state. Upon exit from DPD the device will have the same default settings that exist after Power-On Reset. See Section 10.8.2 Deep Power-Down.

10.7 Power-Off with Hardware Data Protection

The memory is considered to be powered off when the core power supply (V_{CC}) drops below the lock-out voltage (V_{LKO}). When V_{CC} is below V_{LKO}, the entire memory array is protected against a program or erase operation. This ensures that no spurious alteration of the memory content can occur during power transition. During a power supply transition down to Power-Off, $V_{CC}Q$ should remain less than or equal to V_{CC}.

If V_{CC} goes below V_{RST} (Min) then returns above V_{RST} (Min) to V_{CC} minimum, the Power-On Reset interface state is entered and the EAC starts the Cold Reset Embedded Algorithm.

10.8 Power Conservation Modes

10.8.1 Active Clock Stop

The Active Clock Stop state reduces device interface energy consumption to the I_{CC6} level during the data transfer portion of a read or write operation. The device automatically enables this state when clock remains stable for t_{ACC} + 30 ns. While in Active Clock Stop state, read data is latched and always driven onto the data bus. I_{CC6} shown in Section 10.5 DC Characteristics (CMOS Compatible).

Active Clock Stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be LOW throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 ns. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. Clock can be stopped during any portion of the active transaction as long as it is in the LOW state. Note that it is recommended to avoid stopping the clock during register access.

10.8.2 Deep Power-Down

In the Deep Power-Down (DPD) Mode current consumption is driven to the lowest level. The DPD Mode must be entered while the device is in the Standby state while not in an ASO. DPD is entered using the DPD Entry command sequence (See Table 40. Command Definitions). During the t_{DPDIN} period the device will ignore command sequences (read and write transactions will not be processed).

Exiting the DPD Mode is accomplished with the assertion of DPD Entry command sequence. During the t_{DPDOUT} period the device will ignore command sequences (read and write transactions will not be processed) and RWDS will not toggle during an attempted read transaction.

During the t_{DPDIN} period the device will ignore CS#. Entering DPD mode is not interrupted or aborted by a command sequence. Exiting DPD mode must be done after satisfying t_{DPDIN}.

Driving the RESET# input Low (for the minimum t_{RP} time) will also cause the device to exit the DPD Mode. The device will take t_{DPDOUT} to return to the Standby state. Entering DPD mode is aborted by driving the RESET# input Low (for the minimum t_{RP} time) during t_{DPDIN}.

Upon exit from DPD mode the device will have the same default settings that exist after Power-On Reset.

Table 49. DPD Mode Entry and Exit Timing

Symbol	Parameter	Min	Max	Unit
t_{DPDIN}	Deep Power-Down CR[15]=0 register write to DPD power level	10	–	µs
t_{DPDOUT}	Deep Power-Down to Standby wakeup time	–	300	µs

Figure 25. Deep Power Down Entry Timing

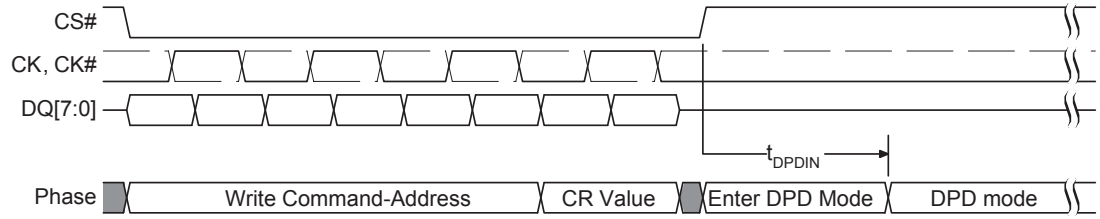


Figure 26. Deep Power Down CS# Exit Timing

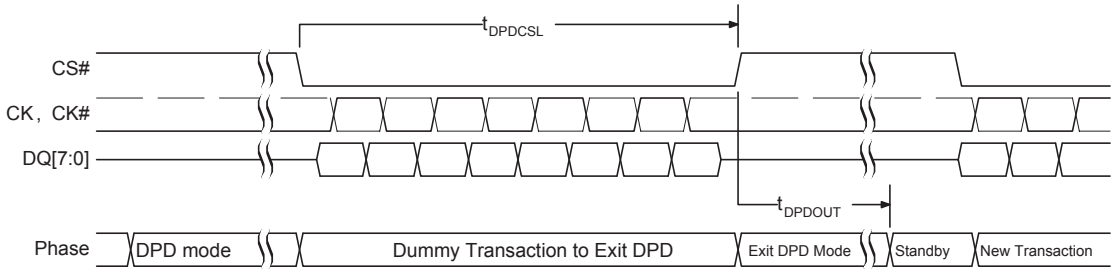
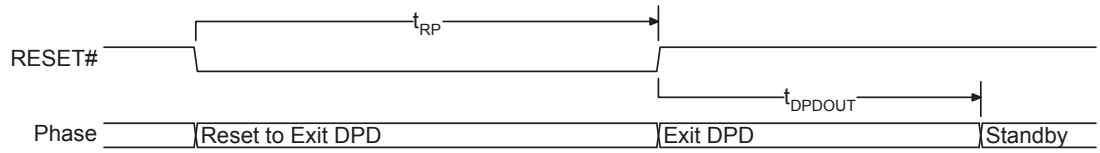


Figure 27. Deep Power Down RESET# Exit Timing



11. Timing Specifications

The following section describes HyperFlash device dependent aspects of timing specifications.

11.1 AC Test Conditions

Figure 28. Test Setup

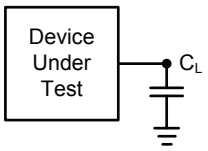


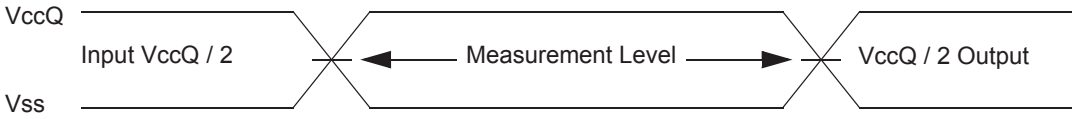
Table 50. Test Specification

Parameter	All Speeds	Units
Output Load Capacitance, C_L	20	pF
Minimum Input Rise and Fall Slew Rates (Note 1)	2.0	V/ns
Input Pulse Levels	0.0-V_{CCQ}	V
Input timing measurement reference levels	$V_{CCQ}/2$	V
Output timing measurement reference levels	$V_{CCQ}/2$	V

Notes:

1. *All AC timings assume an input slew rate of 2V/ns. CK/CK# differential slew rate of at least 4V/ns.*
2. *Input and output timing is referenced to $V_{CC}Q/2$ or to the crossing of CK/CK#.*

Figure 29. Input Waveforms and Measurement Levels



Note:

1. *Input timings for the differential CK/CK# pair are measured from clock crossings.*

11.2 AC Characteristics

11.2.1 CLK Characteristics

Figure 30. Clock Characteristics

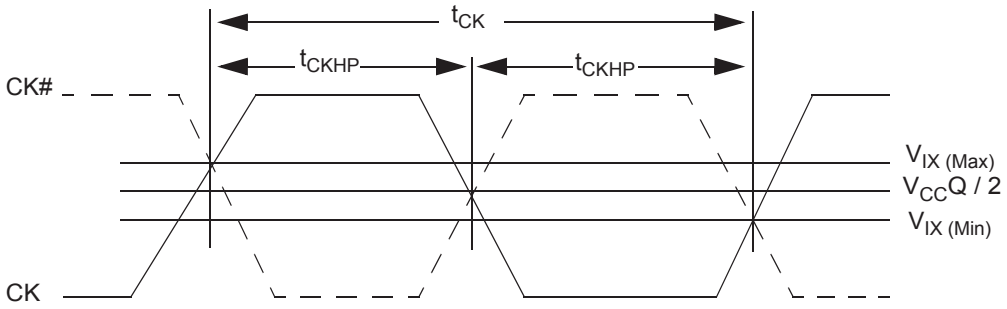


Table 51. Clock Timings

Parameter	Symbol	166 MHz		133 MHz		100 MHz		50 MHz (2)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CK Period	t_{CK}	6	–	7.5	–	10	–	20	–	ns
CK Half Period - Duty Cycle	t_{CKHP}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
CK Half Period at Frequency Min = 0.45 t_{CK} Min Max = 0.55 t_{CK} Min	t_{CKHP}	2.7	3.3	3.375	4.125	4.5	5.5	9	11	ns

Notes:

1. *Clock jitter of ±5% is permitted.*
2. *50 MHz timings are only relevant when a burst write is used to load data during a HyperFlash Word Program command.*
3. *CK# is only used on the 1.8V device and is shown as a dashed waveform.*

Table 52. Clock AC/DC Electrical Characteristics

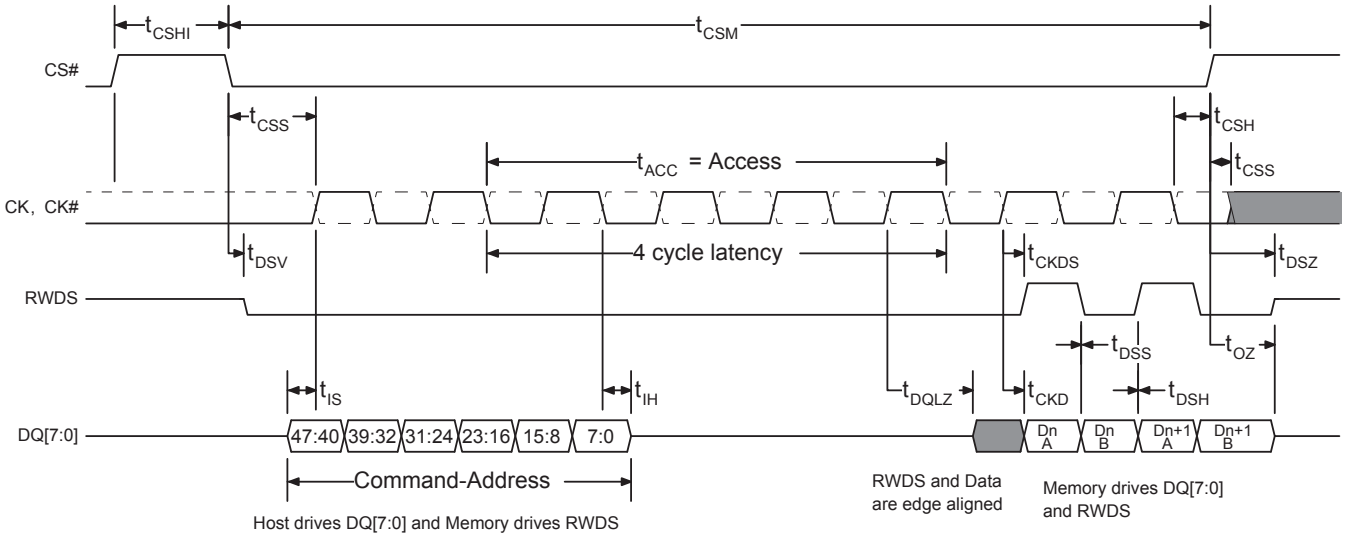
Parameter	Symbol	Min	Max	Unit
DC Input Voltage	V_{IN}	-0.3	$V_{CC}Q$+ 0.3	V
DC Input Differential Voltage	$V_{ID(DC)}$	$V_{CC}Q$x 0.4	$V_{CC}Q$+ 0.6	V
AC Input Differential Voltage	$V_{ID(AC)}$	$V_{CC}Q$x 0.6	$V_{CC}Q$ + 0.6	V
AC Differential Crossing Voltage	V_{IX}	$V_{CC}Q$ x 0.4	$V_{CC}Q$ x 0.6	V

Notes:

1. *CK and CK# input slew rate must be >=1V/ns (2V/ns if measured differentially).*
2. *V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.*
3. *The value of VIX is expected to equal $V_{CC}Q$/2 of the transmitting device and must track variations in the DC level of $V_{CC}Q$.*

11.2.2 Read Transaction Diagrams

Figure 31. Read Timing Diagram



11.2.3 Read AC Parameters

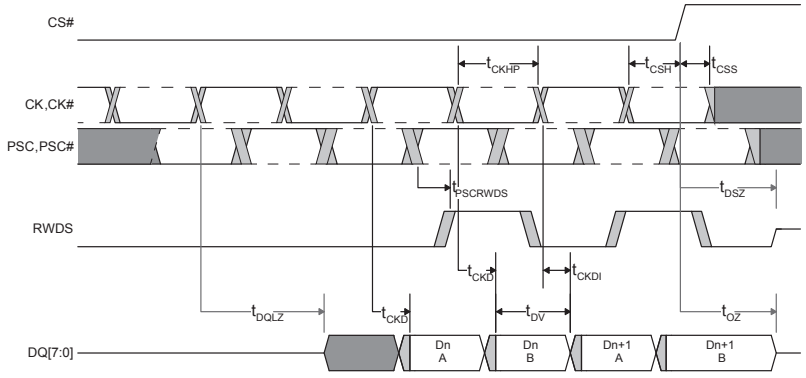
Table 53. HyperBus 1.8V/3.0V Device Common Read Timing Parameters

Parameter	Symbol	166 MHz		133 MHz		100 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Chip Select High Between Transactions	t_{CSHI}	6.00	–	7.50	–	10.00	–	ns
Chip Select Setup to next CK Rising Edge	t_{CSS}	3.00	–	3.00	–	3.00	–	ns
Data Strobe Valid	t_{DSV}	–	12.00	–	12.00	–	12.00	ns
Input Setup	t_{IS}	0.60	–	0.80	–	1.00	–	ns
Input Hold	t_{IH}	0.60	–	0.80	–	1.00	–	ns
HyperFlash Read Initial Access Time	t_{ACC}	–	96.00	–	96.00	–	96.00	ns
Clock to DQs Low Z	t_{DQLZ}	0	–	0		0	–	ns
CK transition to DQ Valid	t_{CKD}	1.00	5.50	1.00	5.50	1.00	5.50	ns
CK transition to DQ Invalid	t_{CKDI}	0	4.60	0	.50	0	.30	ns
Data Valid (t_{DV} *min = the lessor of:* t_{CKHP} *min -* t_{CKD} *max +* t_{CKDI} *max*) or (t_{CKHP} *min -* t_{CKD} *min +* t_{CKDI} *min*)	t_{DV}	1.70	–	2.37	–	3.30	–	ns
CK transition to RWDS valid	t_{CKDS}	1.00	5.50	1.00	5.50	1.00	5.50	ns
RWDS transition to DQ Valid	t_{DSS}	-0.45	+0.45	-0.60	+0.60	-0.80	+0.80	ns
RWDS transition to DQ Invalid	t_{DSH}	-0.45	+0.45	-0.60	+0.60	-0.80	+0.80	ns
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	0		0	–	ns
Chip Select Inactive to RWDS High-Z	t_{DSZ}	–	6.00	–	.00	–	.00	ns
Chip Select Inactive to DQ High-Z	t_{OZ}	–	6.00	–	.00	–	.00	ns

Note:

1. *A HyperBus device operates correctly with the t_{CSH} value shown, however, CS# must generally remain driven Low (active) by the HyperBus master longer, so that data remains valid long enough to account for t_{CKD}, t_{CKDS}, and the master interface phase shifting of RWDS to capture the last data transfer from the DQ signals. The HyperBus master will need to drive CS# Low for one or more additional clock periods to ensure capture of valid data from the last desired data transfer.*

Figure 32. DCARS Data Valid Timing



RWDS and Data are driven by the memory

Notes:

1. *CK# and PSC# are optional and shown as dashed line waveforms.*
2. *The delay (phase shift) from CK to PSC is controlled by the HyperBus master interface (Host) and is generally between 40 and 140 degrees in order to place the RWDS edge within the data valid window with sufficient set-up and hold time of data to RWDS. The requirements for data set-up and hold time to RWDS are determined by the HyperBus master interface design and are not addressed by the HyperBus slave timing parameters.*
3. *The HyperBus timing parameters of t_{CKD}, and t_{CKDI} define the beginning and end position of the data valid period. The t_{CKD} and t_{CKDI} values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.*

Table 54. DCARS Read Timings (@ 3.0 V)

Parameter	Symbol	100 MHz		Unit
		Min	Max	
HyperFlash PSC transition to RWDS transition	$t_{PSCRWDS}$	1	6.5	ns
Time delta between CK to DQ valid and PSC to RWDS	$t_{PSCRWDS} - t_{CKD}$	-1.0	+0.5	ns

Note:
1. Sampled, not 100% tested.

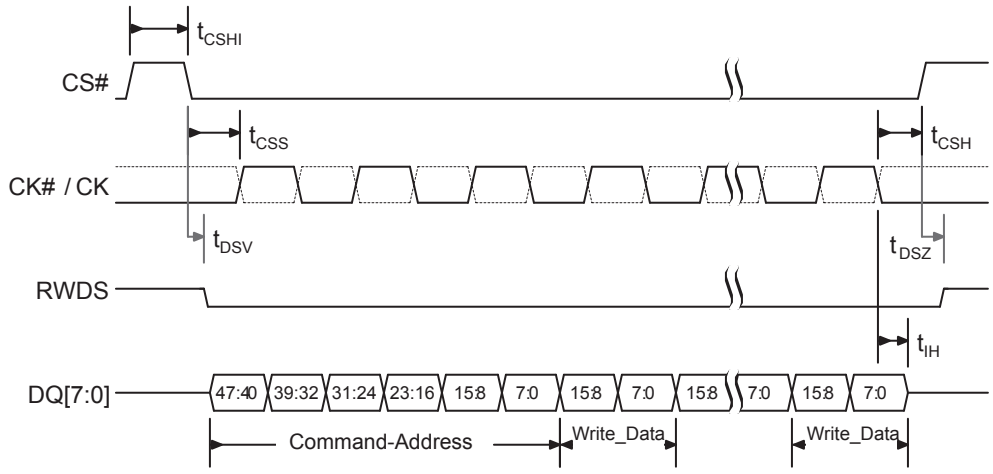
Table 55. DCARS Read Timings (@ 1.8 V)

Parameter	Symbol	133 MHz		100 MHz		Unit
		Min	Max	Min	Max	
HyperFlash PSC transition to RWDS transition	$t_{PSCRWDS}$	1	5.5	1	5.5	ns
Time delta between CK to DQ valid and PSC to RWDS	$t_{PSCRWDS} - t_{CKD}$	-1.0	+0.5	-1.0	+0.5	ns

Note:
1. Sampled, not 100% tested.

11.2.4 Word Programming with Multiple Word Burst Data Load

Figure 33. Burst Write During Load of Multiple Words During a Word Program Command Timing Diagram



Host drives DQ[7:0] with Command-Address and Write Data

Notes:
1. Transactions must be initiated with CK = Low and CK# = High. CS# must return High before a new transaction is initiated.
2. HyperFlash memory drives RWDS Low during write while CS# is Low.
3. Burst Write operations are not allowed while in an ASO state.
4. Burst Write operations are only allowed while loading multiple words during a Word Program command.
5. Burst write operations are linear only, no wrapped burst write capability is supported.
6. CK# is only used on the 1.8V device.

11.2.5 Write AC Parameters

Table 56. HyperFlash 1.8V/3.0V Device Common Write Timing Parameters

Parameter	Symbol	166 MHz		133 MHz		100 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Chip Select High Between Transactions	t_{CSHI}	6.00	–	.50	–	10.00	–	ns
Chip Select Setup to next CK Rising Edge	t_{CSS}	3.00	–	3.00	–	3.00	–	ns
Data Strobe Valid	t_{DSV}	–	12.00	–	12.00	–	12.00	ns
Input Setup	t_{IS}	0.60	–	0.80	–	1.00	–	ns
Input Hold	t_{IH}	0.60	–	0.80	–	1.00	–	ns
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–		–	0	–	ns
Chip Select Inactive or clock to RWDS High-Z	t_{DSZ}	–	6.00	–	6.00	–	.00	ns

Table 57. Burst Write During Load of Multiple Words During a Word Program Command Timings

Parameter	Symbol	50 MHz (2)		Unit
		Min	Max	
Operating Frequency for Burst Write			50	MHz
Chip Select Setup to next CK Rising Edge	t_{CSS}	3	–	ns
Chip Select Active to RWDS Valid (Low)	t_{DSV}	–	8	ns
Input Setup	t_{IS}	1.0	–	ns
Input Hold	t_{IH}	1.0	–	ns
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	ns
Chip Select Inactive to RWDS High-Z	t_{DSZ}	–	6	ns
Chip Select High Between Operations	t_{CSHI}	10.0	–	ns

Notes:

1. *Sampled, not 100% tested.*
2. *50 MHz timings are only required when using a burst write during a Word Program command.*

12. Embedded Algorithm Performance

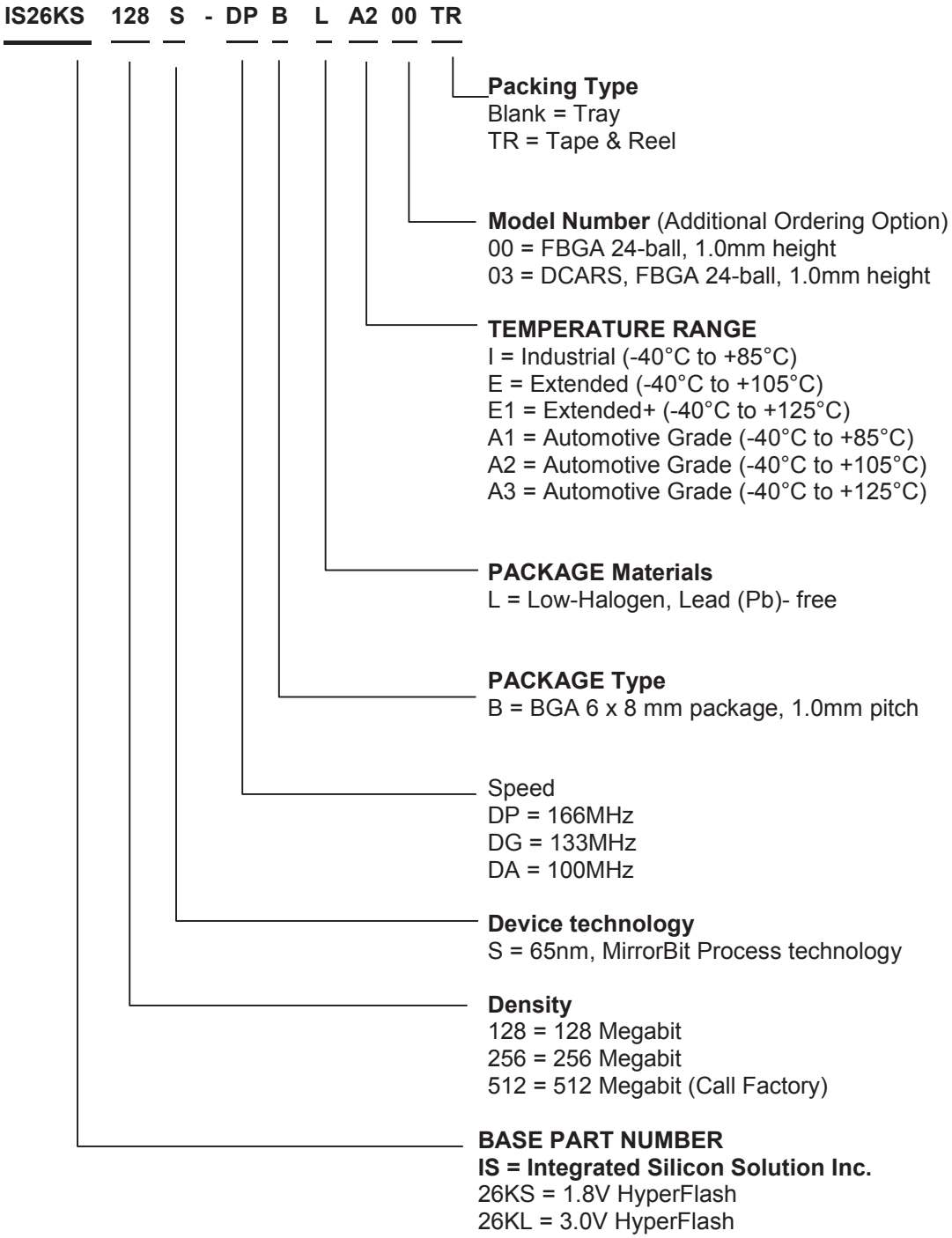
Table 58. Embedded Algorithm Characteristics

Parameter	Min	Typ (1)	Max (2)	Unit	Comments
Sector Erase Time 256-Kbyte	–	930	2900	ms	Includes pre-programming prior to erasure (4)
Parameter Sector Erase Time 4-Kbyte	–	240	725	ms	
Chip Erase Time (128 Mb)		55	115	s	
Chip Erase Time (256 Mb)	–	110	231	s	
Chip Erase Time (512 Mb)	–	220	462	s	
Single Word Programming Time	–	270	1000	µs	Word Programming Command Sequence
Half-page (16-byte) Buffered Programming Time	–	270	1000	µs	Buffered Programming Command Sequence
Buffer Programming Time (full 512-byte)	–	475	2000	µs	
Erase Suspend / Erase Resume (t_{ESL})	–		50	µs	
Program Suspend / Program Resume (t_{PSL})	–		50	µs	
Erase Resume to next Erase Suspend (t_{ERS})	–	100			Minimum of 60 ns but ≥ typical periods are needed for Erase to progress to completion
Program Resume to next Program Suspend (t_{PRS})	–	100		µs	Minimum of 60 ns but ≥ typical periods are needed for Program to progress to completion
Blank Check (256-kB Sector)	–	15	17	ms	
NOP (Number of Program-operations, per Line)	–		256		Industrial Temperature
	–		32		Industrial Plus Temperature Only a single program operation on each 8-word (16-byte) half-page
Evaluate Erase Status Time (t_{EES})	–	70	100	µs	
Password Comparison Time (t_{PSWD})	80	100	120	µs	
CRC Suspend / CRC Resume (t_{CRCSL})	—		25	µs	
CRC Resume to next CRC Suspend (t_{CRCRS})	—	5		µs	Minimum of 60 ns but ≥ typical periods are needed for the CRC calculation to progress to completion
CRC Calculation Setup Time (t_{CRC_SETUP})	—	10	—	µs	
CRC Calculation Rate	60	65		MB/s	Calculation rate over a large (>1024-byte) block of data

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, (1.8V or 3.0V) V_{CC}, 10,000 cycle, and a checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = (1.70V or 2.7V), 100,000 cycles, and a random data pattern.*
3. *Effective write buffer specification is based upon a 512-byte write buffer operation.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 0000h before Sector and Chip erasure.*
5. *System-level overhead is the time required to execute the bus-cycle sequence for the program command. See Table 40. Command Definitions for further information on command definitions.*

13. ORDERING Rule for HyperFlash



14. ORDERING INFROMATION

256Mb HyperFlash

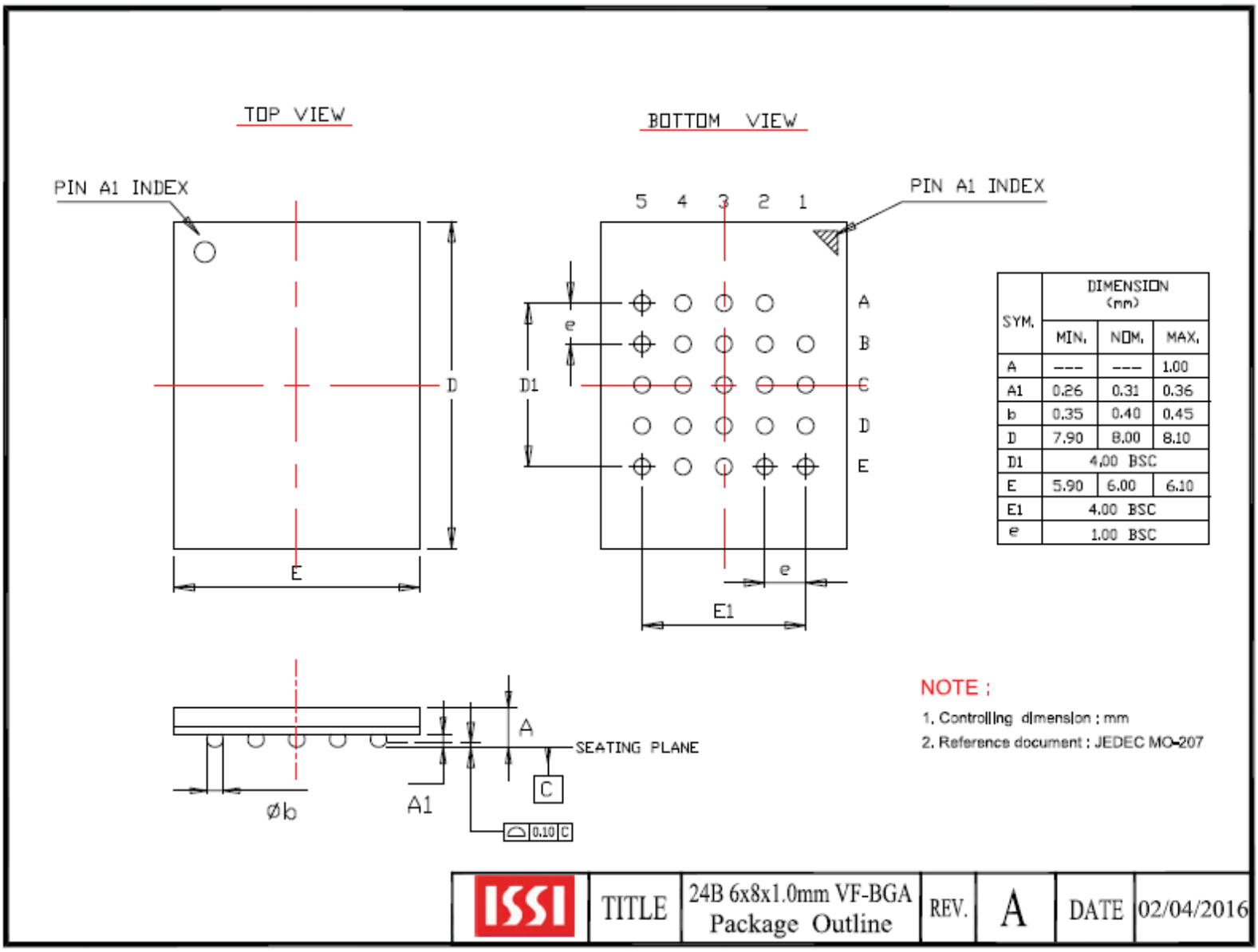
Density	Ordering Part Number	Voltage	Speed (MHz)	Package	Temperature	Remarks
256Mb	IS26KS256S-DPBLI00	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KS256S-DPBLE00	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KS256S-DPBLE100	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KS256S-DPBLA100	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KS256S-DPBLA200	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KS256S-DPBLA300	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive
	IS26KL256S-DABLI00	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KL256S-DABLE00	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KL256S-DABLE100	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KL256S-DABLA100	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KL256S-DABLA200	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KL256S-DABLA300	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive
256Mb, DCARS	IS26KS256S-DGBLI03	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KS256S-DGBLE03	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KS256S-DGBLE103	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KS256S-DGBLA103	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KS256S-DGBLA203	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KS256S-DGBLA303	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive
	IS26KL256S-DABLI03	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KL256S-DABLE03	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KL256S-DABLE103	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KL256S-DABLA103	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KL256S-DABLA203	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KL256S-DABLA303	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive

128Mb HyperFlash

Density	Ordering Part Number	Voltage	Speed (MHz)	Package	Temperature	Remarks
128Mb	IS26KS128S-DPBLI00	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KS128S-DPBLE00	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KS128S-DPBLE100	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KS128S-DPBLA100	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KS128S-DPBLA200	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KS128S-DPBLA300	1.8V	166	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive
	IS26KL128S-DABLI00	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KL128S-DABLE00	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KL128S-DABLE100	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KL128S-DABLA100	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KL128S-DABLA200	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KL128S-DABLA300	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive
128Mb, DCARS	IS26KS128S-DGBLI03	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KS128S-DGBLE03	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KS128S-DGBLE103	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KS128S-DGBLA103	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KS128S-DGBLA203	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KS128S-DGBLA303	1.8V	133	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive
	IS26KL128S-DABLI03	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	
	IS26KL128S-DABLE03	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	
	IS26KL128S-DABLE103	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	
	IS26KL128S-DABLA103	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 85°C	Automotive
	IS26KL128S-DABLA203	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 105°C	Automotive
	IS26KL128S-DABLA303	3.0V	100	24 VF-BGA, Pb-free & Halogen-free	-40 to 125°C	Automotive

Note:
1. A1, A2, A3 : Meets AEC-Q100 requirements with PPAP

15. PACKAGE DRAWING



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

NOTE :
1. Controlling dimension : mm
2. Reference document : JEDEC MO-207

	TITLE	24B 6x8x1.0mm VF-BGA Package Outline	REV.	A	DATE	02/04/2016