IS66WVO64M8DALL/BLL
IS67WVO64M8DALL/BLL

512Mb OctalRAM

1.8V/3.0V SERIAL PSRAM MEMORY WITH 200MHZ DTR OPI (OCTAL PERIPHERAL INTERFACE) PROTOCOL

PRELIMINARY DATA SHEET

512Mb OctalRAM

DDP (Dual Die Package) SERIAL PSRAM MEMORY WITH 200MHz DTR OPI (Octal Peripheral Interface) Protocol

FEATURES

- **Industry Standard Serial Interface**
  - Octal Peripheral Interface (OPI) Protocol
  - Low Signal Counts :11 Signal pins (CS#, SCLK, DQSM, SIO0~SIO7)

- **High Performance**
  - Up to 400MB/s
  - Double Transfer Rate (DTR) Operation
  - 200MHz (400MB/s) at 1.8V VCC
  - 166MHz (332MB/s) at 3.0V VCC
  - Source Synchronous Output signal during Read Operation (DQSM)
  - Data Mask during Write Operation (DQSM)
  - Configurable Latency for Read/Write Operation)
  - Supports Fixed Latency mode only
  - Configurable Drive Strength
  - Supports Wrapped Burst mode and Continuous Burst mode
  - Hidden Refresh

- **Burst Operation**
  - Configurable Wrapped Burst Length : 16, 32, 64, and 128
  - Word Order Burst Sequence
  - Continuous Burst Operation:
    Continues Read operation until the end of array address
    Continues Write operation even after the end of array address

- **Low Power Consumption**
  - Single 1.7V to 1.95V Voltage Supply
  - Single 2.7V to 3.6V Voltage Supply
  - 1400 µA Standby Current (typ.)

- **Hardware Features**
  - **SCLK Input**: Serial clock input
  - **SIO0 - SIO7**:
    Serial Data Input or Serial Data Output
  - **DQSM**:
    - Output during command, address transactions as Refresh Collision Indicator
    - Output during read data transactions as Read Data Strobe
    - Input during write data transactions as Write Data Mask
  - **RESET#:** Hardware Reset pin

- **Temperature Grades**
  - Industrial: -40°C to +85°C
  - Auto (A2) Grade: -40°C to +105°C

- **Industry Standard PACKAGE**
  - B = 24-ball TFBGA 6x8mm 5x5 Array
  - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

GENERAL DESCRIPTION

The IS66/67WVO64M8DALL/BLL are 512Mb Dual Die Package memory device containing two units of 256Mb Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 64M words by 8 bits.

The device supports Octal Peripheral Interface (Address, Command, and Data through 8 SIO pins), Very Low Signal Count (11 signal pins; SCLK, CS#, DQSM, and 8 SIOs), Hidden Refresh Operation, and Automotive temperature (A2, -40°C to +105°C) operation.

Due to DTR operation, minimum transferred data size is word (16 bits) base instead of byte (8 bits) base.

PERFORMANCE SUMMARY

Read / Write Operation	
Maximum Clock Rate at 3.0V VCC/VCCQ	166 MHz
Maximum Clock Rate at 1.8V VCC/VCCQ	200 MHz

Maximum Current Consumption		
VCC Active Read Current	3V	40 mA
	1.8V	35 mA
VCC Active Write Current	3V	35 mA
	1.8V	30 mA
Standby (CS# = High, 105°C)	3V	1800 uA
	1.8V	1800 uA

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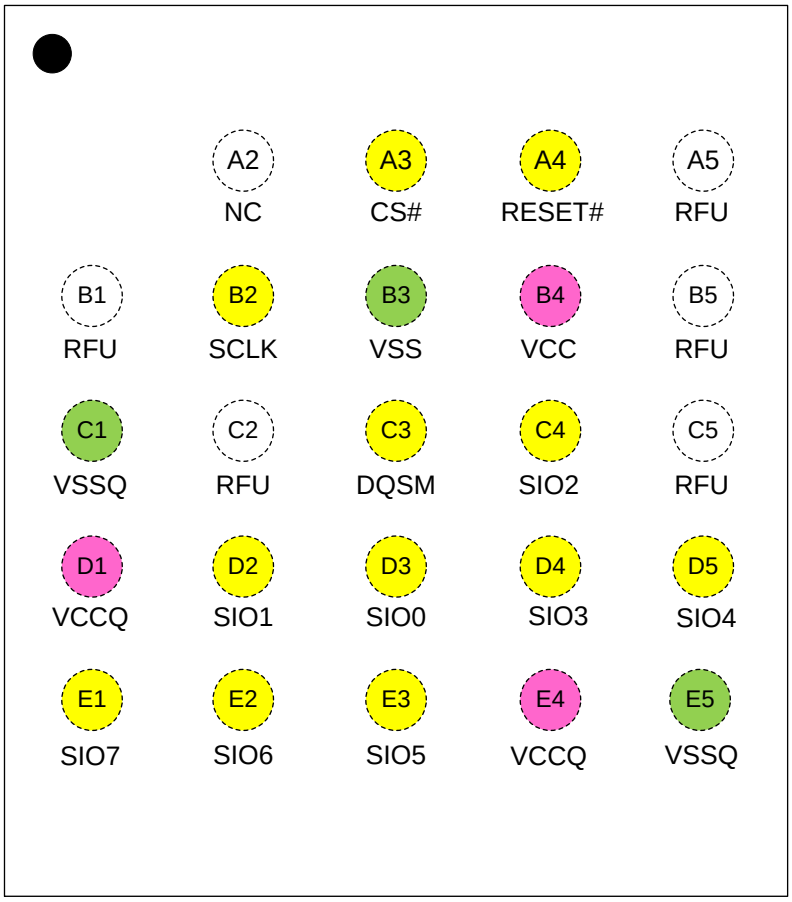
1. PIN CONFIGURATION

24-ball TFBGA (5x5 ball array)

Top View, Balls Facing Down



2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CS#	INPUT	**Chip Select:** Bus transactions are initiated with a High to Low transition. Bus transactions are initiated with a Low to High transition.
DQSM	INPUT/OUTPUT	**Refresh Collision Indicator [2], Data Strobe Signal in Read operation, and Write Data Mask in Write operation:**
RESET#[1]	INPUT	**RESET#:** The RESET# pin is a hardware RESET signal. When RESET# is driven High, the memory is in the normal operating mode. When RESET# is driven Low, the memory enters reset mode and output is High-Z.
SIO0-SIO7	INPUT	**Serial Data Input & Output pins**.
SCLK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
VCC	POWER	**Power Supply**
VCCQ	POWER	**IO Power Supply**
VSS	GROUND	**Ground**
VSSQ	GROUND	**IO Ground**
RFU	Reserved	**RFU:** Reserved for future use: May or may not be connected internally.
NC	Unused	**NC:** No Connect: Not connected internally. The ball may be used in PCB routing.

Notes:

1. **RESET# pin has an internal pull-up.**
2. Contact ISSI MKT for DQSM without Refresh Collision Indicator

3. BLOCK DIAGRAM AND PACKAGE BLOCK DIAGRAM

Figure 3.1 Read Timing Diagram

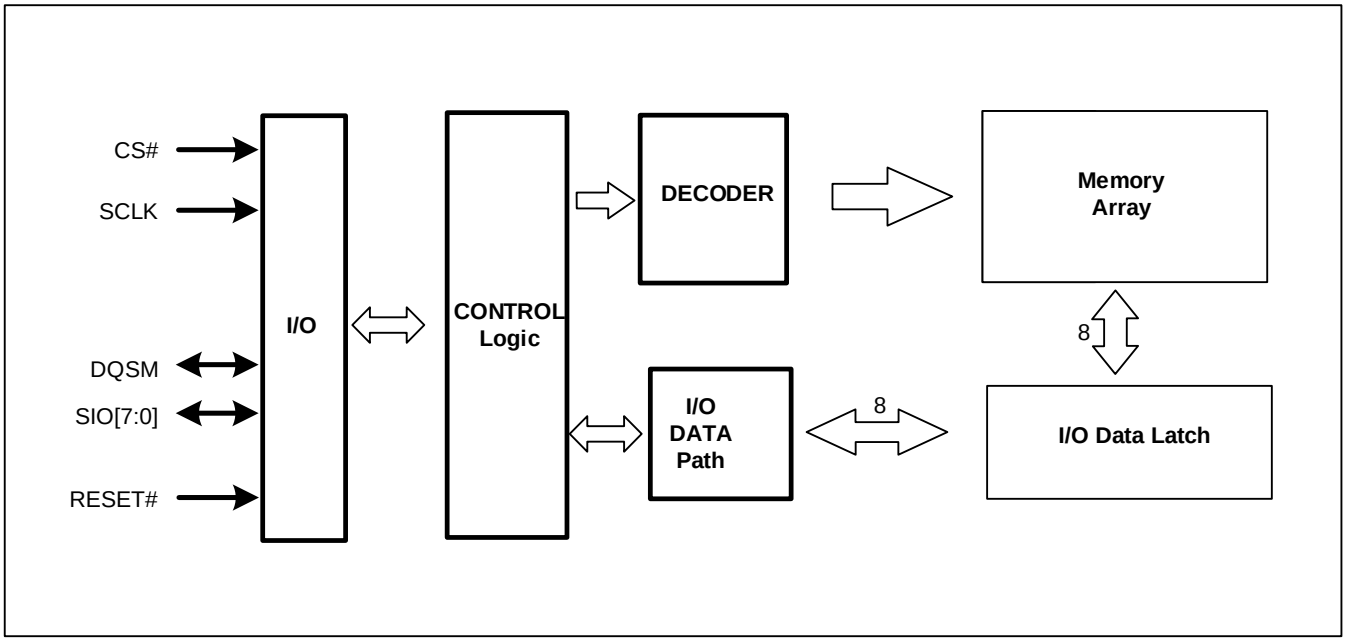
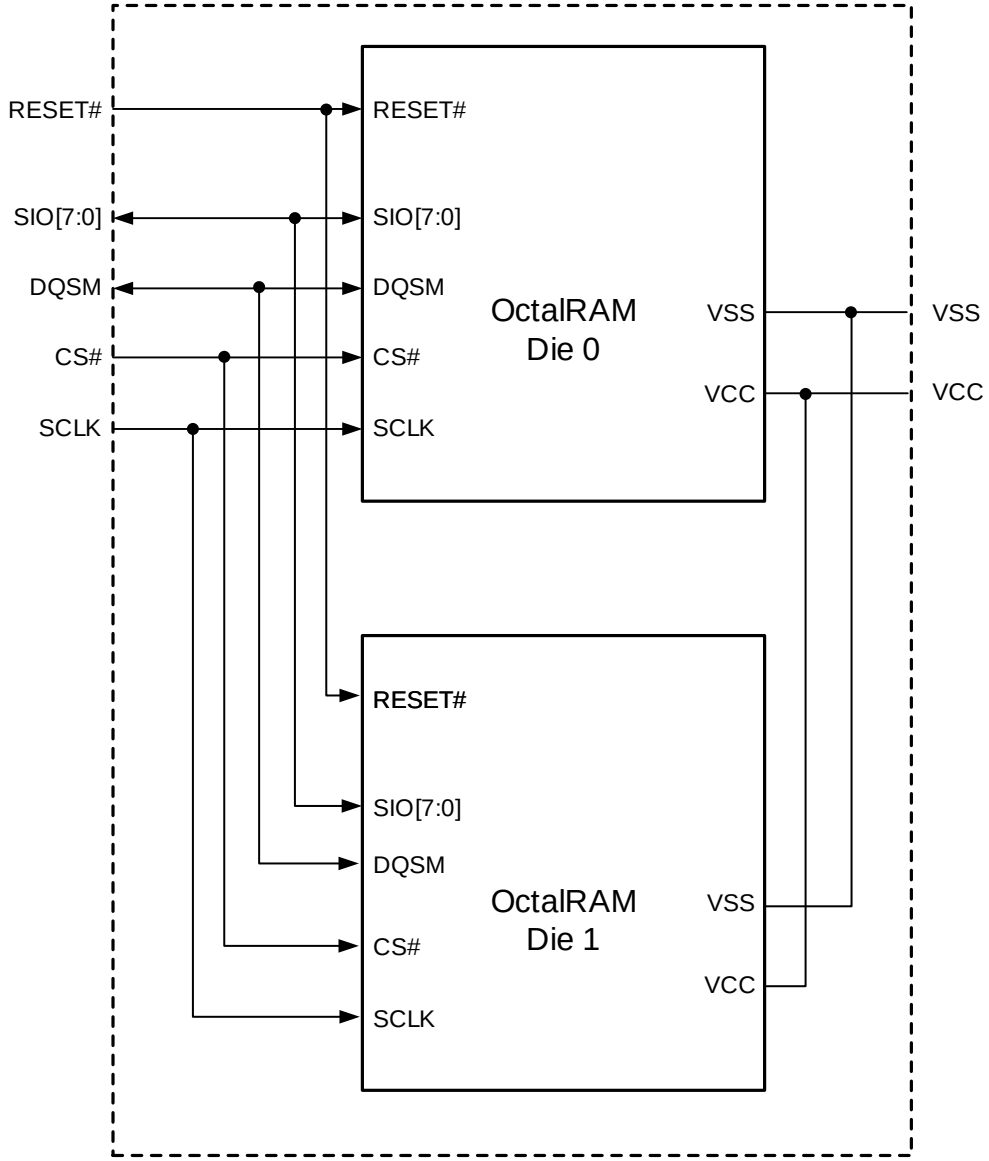


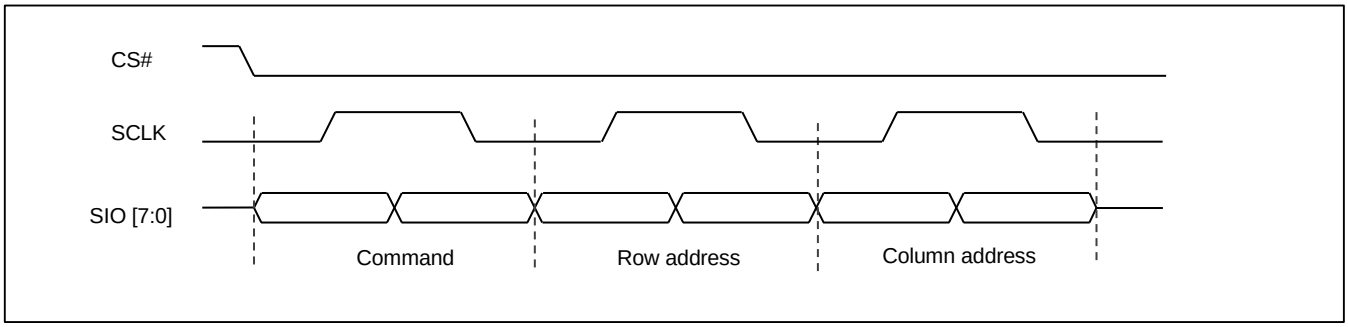
Figure 3.2 Read Timing Diagram



4. COMMAND AND ADDRESS ASSIGNMENTs

The device is serial interface, so all command and address inputs are transferred through SIO pins.

Figure 4.1 Command and Address Cycles



Notes:
1. The figure shows the initial three clock cycles of all operations on the OctalRAM Interface.
2. Command and Address information is "center aligned" with the clock during both Read and Write operations.

Table 4.1 Command / Address bit assignment

Clock	**1st clock**	**2nd clock**		**3rd clock**	
Function	**Command**	**Row address**		**Column address**	
SIO[7]	Command	RA15	RA7	CA9	Reserved
SIO[6]		RA14	RA6	CA8	Reserved
SIO[5]		RA13	RA5	CA7	Reserved
SIO[4]		RA12	RA4	CA6	Reserved
SIO[3]		RA11	RA3	CA5	CA3
SIO[2]		RA10	RA2	CA4	CA2
SIO[1]		RA9	RA1	Reserved	CA1
SIO[0]		RA8	RA0	Reserved	**CA0(3)**

Notes:

1. The 512Mb OctalRAM address assignments:
   - Row Address 15 ~ 0: 64K (16bits), Column Address 9 ~ 0: 1k (10bits), 512Mb density = 64K X 1K X 8 (bits)
2. Data is always transferred in full word increment (word granularity -2 bytes-transfer).
3. Column Address A0 should be always 0.

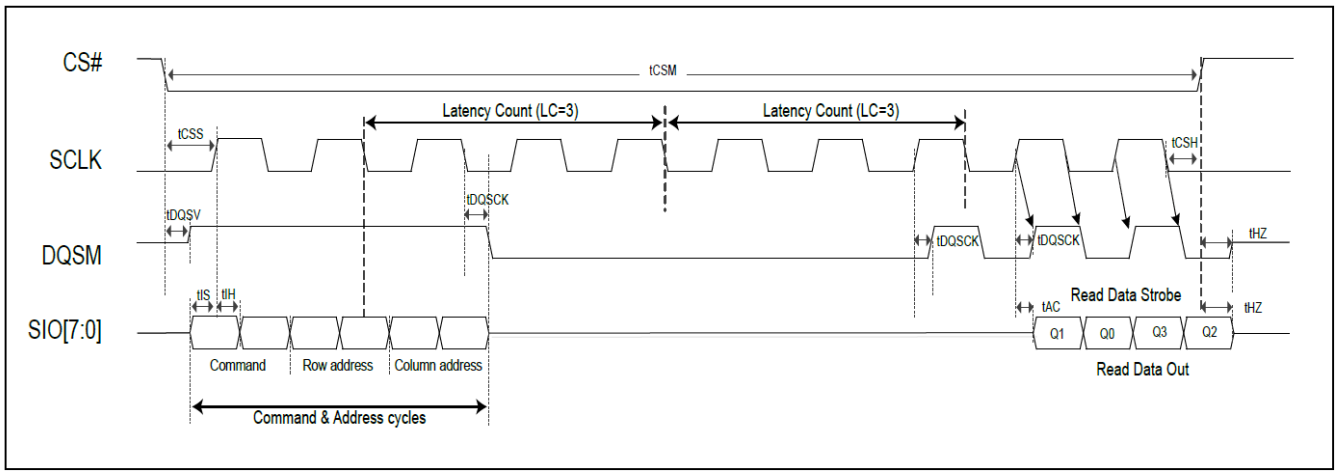
Table 4.2 Command / Address bit assignment

Command		1st clock		2nd clock		3rd clock	
		Command		Row address		Column address	
Memory READ with continuous burst		A0h	00h	RA[15:0]		CA[9:0]	
Memory READ with wrapped burst		80h	00h	RA[15:0]		CA[9:0]	
Memory WRITE with continuous burst		20h	00h	RA[15:0]		CA[9:0]	
Memory WRITE with wrapped burst		00h	00h	RA[15:0]		CA[9:0]	
Identification Register (read only)	Die 0	C0h or E0h	00h	00h	00h	00h	00h
	Die 1	C0h or E0h	00h	80h	00h	00h	00h
Configuration Register READ	Die 0	C0h or E0h	00h	00h	04h	00h	00h
	Die 1	C0h or E0h	00h	80h	04h	00h	00h
Configuration Register WRITE	Die 0	40h or 60h	00h	00h	04h	00h	00h
	Die 1	40h or 60h	00h	80h	04h	00h	00h
Preamble Bit Pattern READ	Die 0	F0h	00h	0xxxh		CA[9:1] Don't care CA[0] Pattern Selection	
	Die 1	F0h	00h	8xxxh			

5. Memory READ/WRITE OPERATIONS

5.1 MEMORY READ OPERATIONS

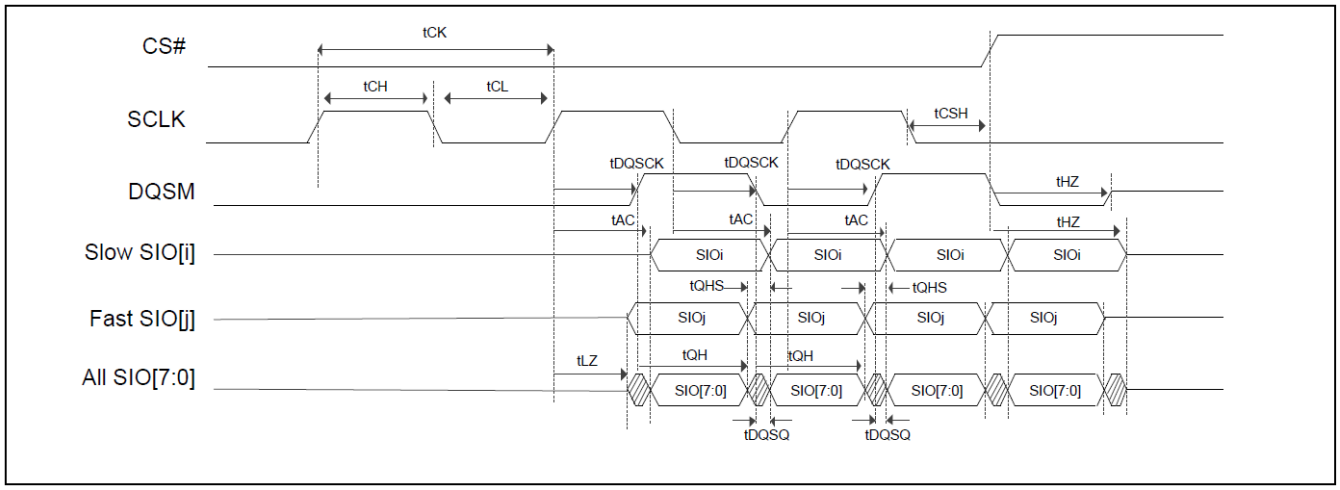
Figure 5.1 Read Timing Diagram – Fixed Latency READ (2LC operation)



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **fixed latency access**.
4. In this Read there is a 2 Latency Count (2LC) for read access.
5. Read access (LC) starts once RA [7:0] is captured.
6. The memory drives DQSM during read cycles.
7. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM.
8. Column address A0 must be 0.
9. **Fixed initial READ access latency outputs the first data at a consistent time regardless of worst-case refresh collisions.**

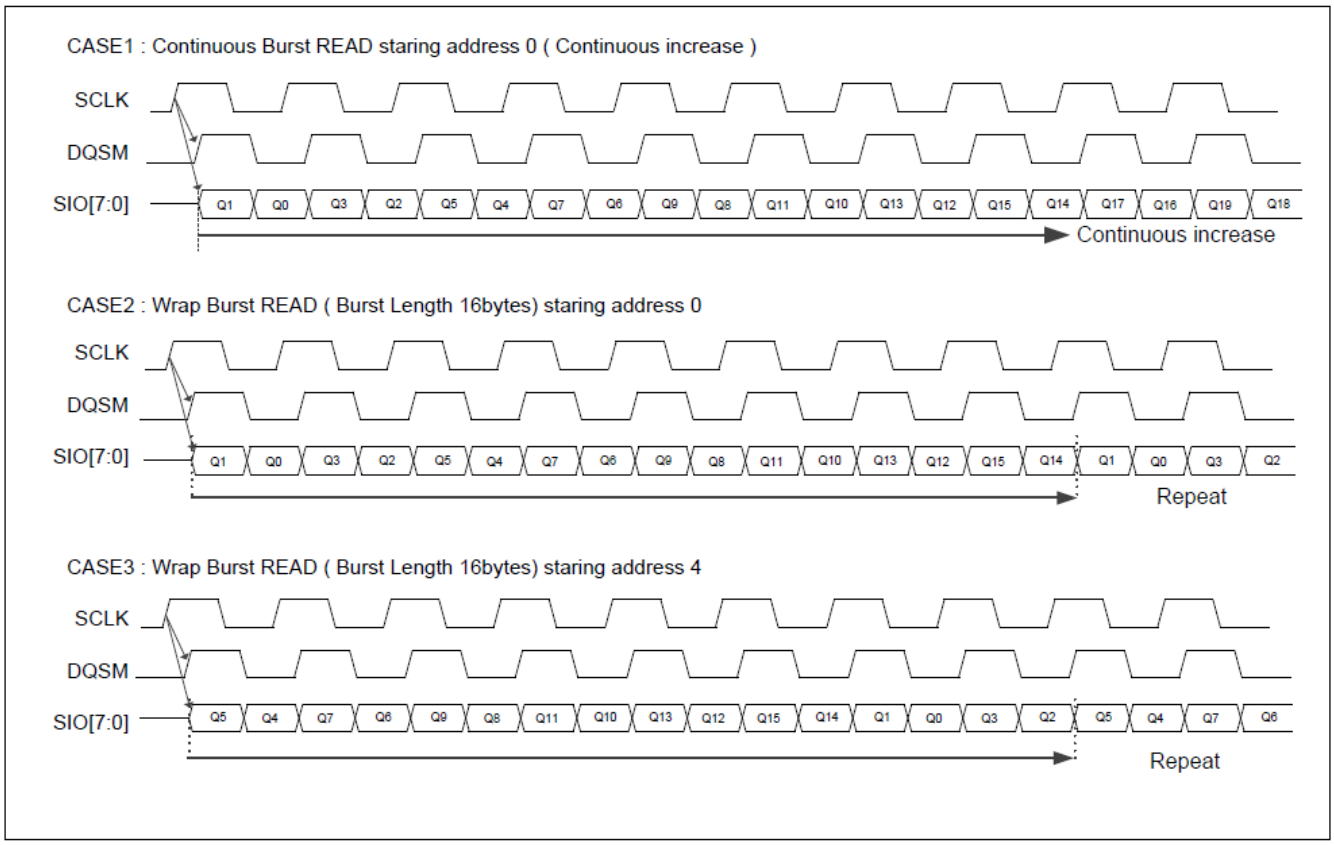
Figure 5.2 Data Valid Timing



Notes:

1. Burst READ data valid timing in detail.
2. tAC defines CLK transition to DQ Valid.
3. tDQSCK defines CLK transition to DQSM Valid.
4. tDQSQ defines DQSM-DQ skew.
5. tQHS defines Data Hold skew factor.
6. tQH defines DQ hold time from DQSM.

Figure 5.3 READ Burst Wrap

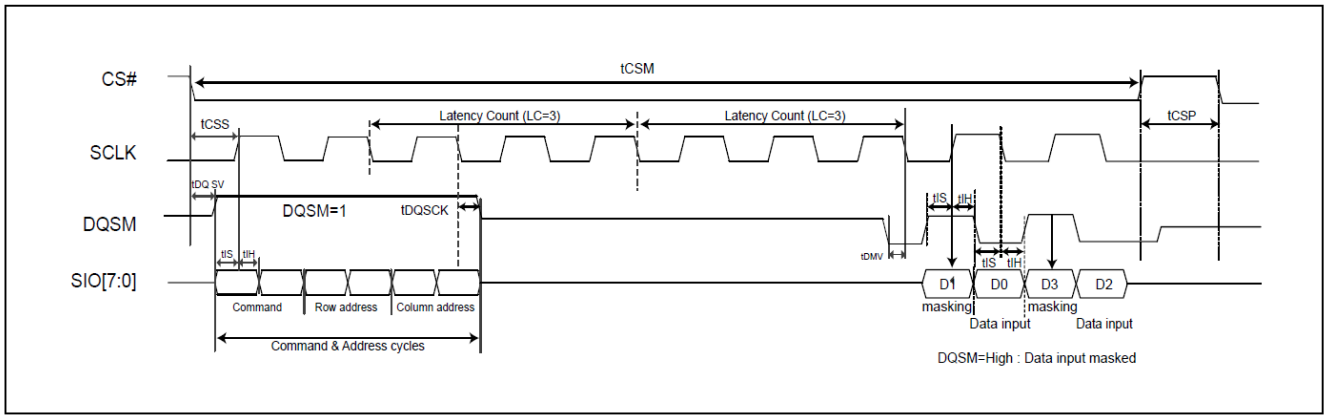


Notes:

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Read operation can be ended at any time by bringing CS# High.
3. Continues Read operation until last address. Continuing beyond last address, undefined data will be available.

5.2 WRITE OPERATIONS

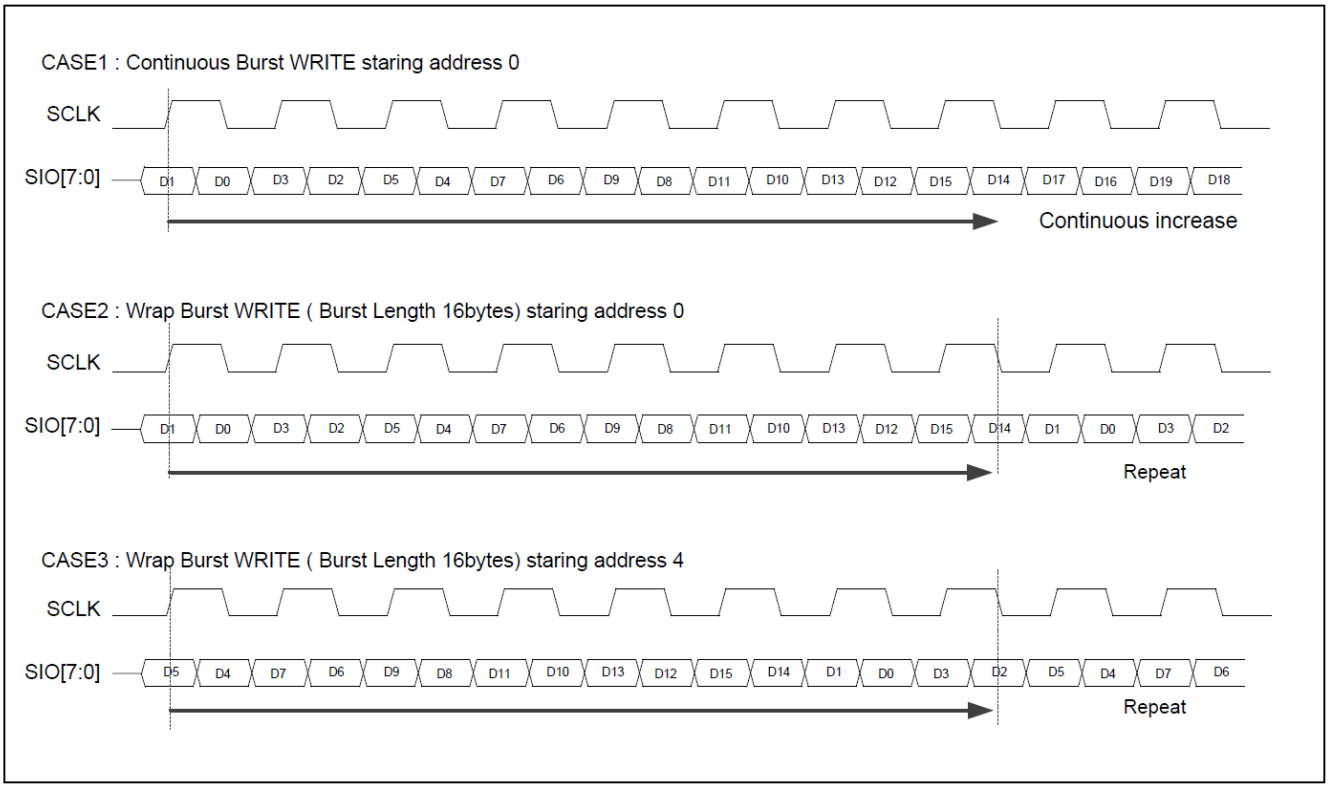
Figure 5.4 Refresh Collision at Fixed Latency WRITE (2LC) / Data Input Masking



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks.
3. Diagram in the figure above is representative of **fixed latency access.**
4. **In this Write there is a latency count (2LC) for WRITE operation**
5. Write access (LC) starts once RA [7:0] is captured.
6. The memory drives DQSM Low during command address cycles and DQSM goes to “Hi-Z” after command address cycles.
7. The system memory controller must drive DQSM to a valid Low before the end of initial latency to provide a data mask preamble time.
   This can be done during the last cycle of LC cycle.
8. During Write data input, data is center aligned with the clock.
9. During Write data input, DQSM indicates whether each data byte is masked with DQSM High or not masked with DQSM Low.
10. D1, D3 are masked.
11. Column address A0 must be 0.

Figure 5.5 WRITE Burst Wrap



Notes:

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Write operation can be ended at any time by bringing CS# High.
3. When continuous burst write reaches the last address in the memory array, continuing the burst will write to the beginning of the address.

5.3 PREAMBLE BIT DATA PATTERN READ OPERATION

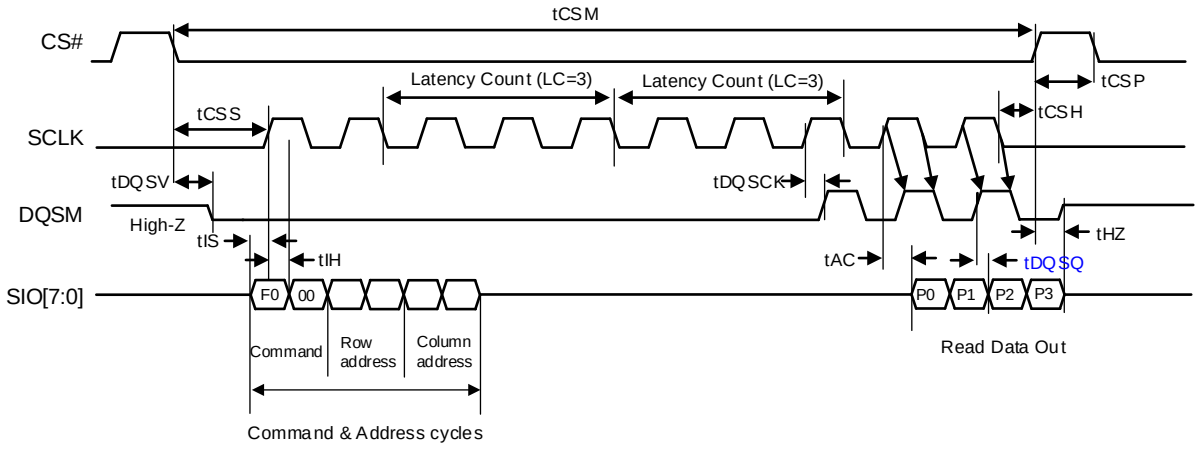
The Preamble Bit Data Pattern READ Operation can improve data capture reliability while the OctalRAM is running in high frequency, while supporting the System/Memory Controller to determine the data output valid windows more easily.

The Preamble Bit is designed as a 16-bits data pattern, it can be output by Preamble Bit READ Command (F0h + 00h). The Row Address and Column Address are “don’t care”, except Column Address A0 is used for selecting the pattern.

Once Preamble Bit feature is enabled, a fixed 16-bits data pattern will output on all SIO pins, according to A0 setting in Column Address. Refer to *"Table 5.1. Preamble Bit Data Pattern SIO assignments"*.

The Latency Count values are defined in configuration register CR [7-4] which is the same as Read timing diagram -1LC operation case.

Figure 5.8 Preamble Bit Data Pattern READ Timing with at Fixed Latency



Notes:

1. Latency Count (LC) = 3 clocks, CR[8]=1 (DQSM 1 clock pre-cycle before Valid READ Data)
2. The memory drives DQSM during the entire Data Learning Pattern Read.
3. The required latency count is device and clock frequency dependent.
4. Column address A0 is used for pattern selection, and Row address RA [15:0] and Column address CA [9:1] are don’t care.

Table 5.1 Preamble Bit Data Pattern SIO assignments

Column Address A0	All SIOs (except SIO3)	SIO3
A0=0	0011 0100 1001 1010	0011 0101 0001 0100
A0=1	0101 0101 0101 0101	0101 0101 0101 0101

5.4 RESET OPERATION

Figure 5.9 RESET Timing

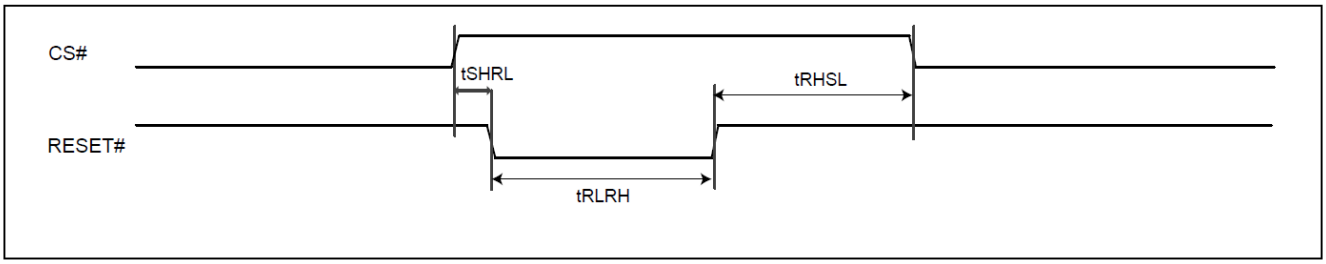
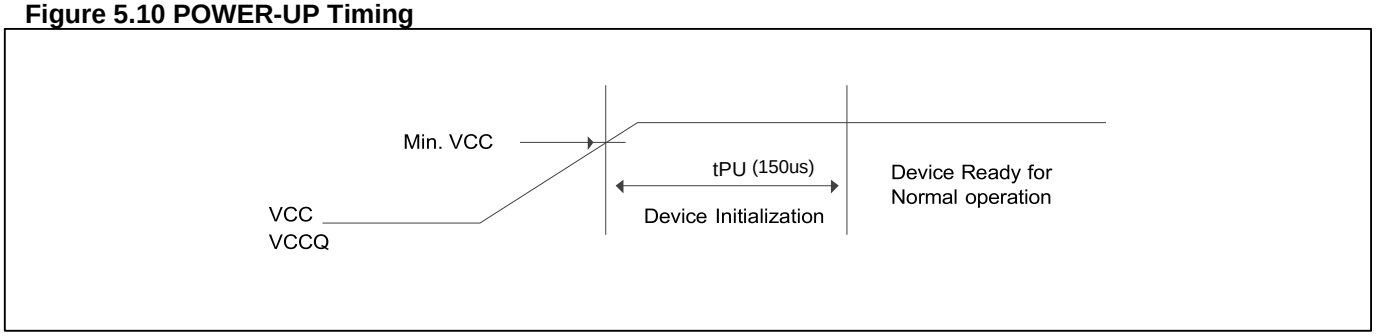


Table 5.2 RESET Timing Parameters

Parameter	Description	Min	Max	Unit
tSHRL	RESET# Low after CS# High	15	-	ns
tRLRH	RESET# Low Pulse width	10	-	us
tRHSL	RESET# High before CS# Low	10	-	us

5.5 POWER-UP INITIALIZATION

Figure 5.10 POWER-UP Timing

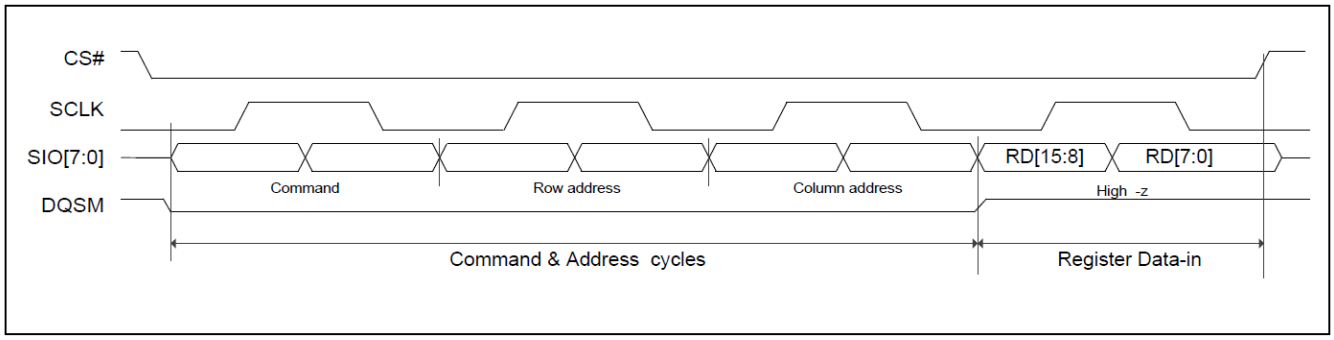


6. REGISTER

The device has 16 bit Configuration Register and ID Register, and they can be accessed by Register Read or Write command.

6.1 REGISTER READ/WRITE OPERATION

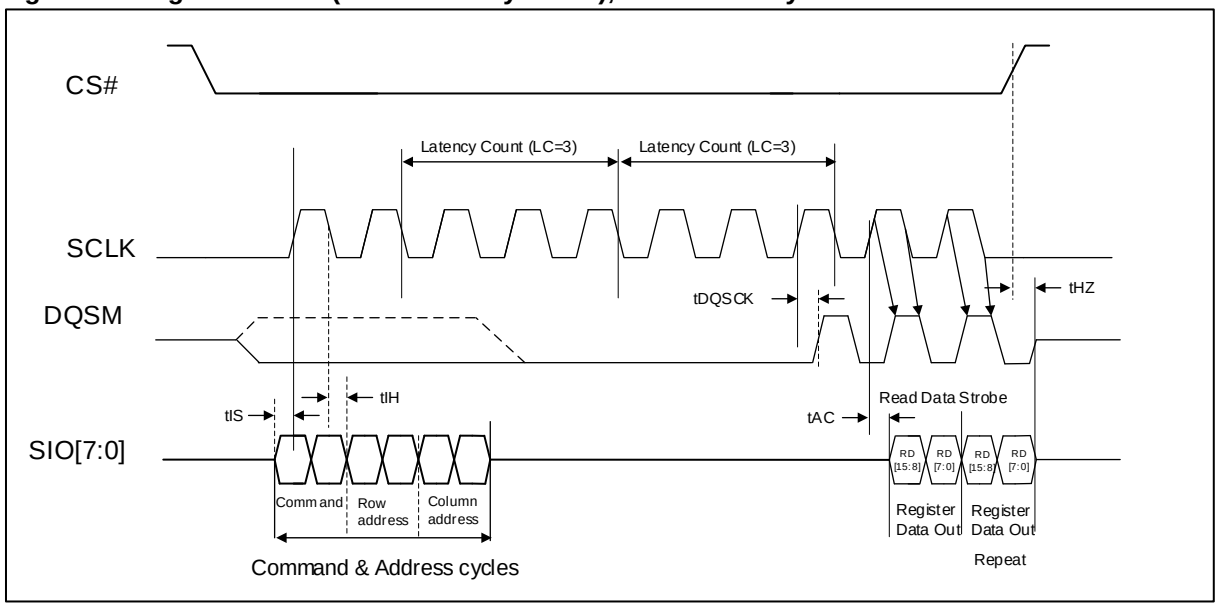
Figure 6.1 Register WRITE at Fixed Latency



Notes:

1. The device drives DQSM "Low or High for Refresh indication" during command address cycles, which must be ignored by host. DQSM goes to "Hi-Z" after command address cycles.
2. The register value is always provided immediately after the Command Address cycles (0 cycle latency)
3. The DQSM signal keep Hi-Z during register data-in cycles. DQSM will be ignored by host and device during entire register write operation.

Figure 6.2 Register READ (Initial Latency = 2LC), Fixed Latency



Notes:

1. The device drives DQSM "Low or High for Refresh indication" during command address cycles, which must be ignored by host. DQSM goes to "Low" after command address cycles until DQSM pre-cycle.
2. Initial Latency is always 2LC for Register Read operation when fixed initial latency is selected by configuration register.
3. DQSM is a read data strobe with register values edge aligned with the transitions of DQSM driven by the device.

6.2 CONFIGURATION REGISTER

The Configuration Register is able to change the defaulted status of the device. The device will be configured after the CR bit is set. 512Mb is a DDP device of two 256Mb, so each die must be programmed and read out individually.

Table 6.1 Configuration Register

Bit	Function	Settings (Binary)
15	Reserved	Set to 1b
14-12	ODS (Output Drive Strength)	Refer to *"Table 6.2. Output Driver Strength Table"*
11-9	Reserved	Set to 000b
8	**DQSM READ Pre-cycle**	**1b - 1 clock** **0b - 0 clock (default)**
7-4	Latency counter	Refer to *"Table 6.3. Latency counter Table"*
3	**Initial Access Latency**	0b - Variable Latency (default) **1b - Fixed Latency** **Note: CR0[3] of each die must be programmed as "1" (Fixed Latency mode)**
2	Reserved	Set to 0b
1-0	Burst Length	00b- 128 bytes 01b- 64 bytes **10b- 32 bytes (default)** 11b- 16 bytes

Table 6.2 Output Driver Strength Table

ODS2	ODS1	ODS0	Description
0	0	0	146 Ohms
0	0	1	76 Ohms
0	1	0	52 Ohms
0	1	1	41 Ohms
1	0	0	34 Ohms
1	0	1	30 Ohms
1	1	0	26 Ohms
1	**1**	**1**	**24 Ohms (Default)**

Table 6.3 Latency counter Table

CR [7:4]	Latency Counter (LC)
0000	3 clocks
0001	4 clocks
0010	5 clocks (default at 3V)
0011	6 clocks
0100	7 clocks
0101	8 clocks (default at 1.8V)
0110~1111	Reserved

6.2.1 WRAPPED BURST LENGTH

Table 6.4 Wrapped Burst Sequences

Command	Configuration Register[1:0]	Burst Type	Wrap Boundary Col. Addr	Start Address (Hex)	Address Sequence (Hex) : Bytes
Read	00	Wrap 128	CA[6:0]	XXXXXX06	07. 06, 09, 08,…. 7F, 7E, 01, 00, 03, 02, 05, 04, 07, 06, …
Write	00	Wrap 128	CA[6:0]	XXXXXX06	07. 06, 09, 08,…. 7F, 7E, 01, 00, 03, 02, 05, 04, 07, 06, …
Read	01	Wrap 64	CA[5:0]	XXXXXX02	03. 02, 05, 04, 07, 06,…. 3D, 3C, 3F, 3E, 01, 00, 03, 02, …
Write	01	Wrap 64	CA[5:0]	XXXXXX02	03. 02, 05, 04, 07, 06,…. 3D, 3C, 3F, 3E, 01, 00, 03, 02, …
Read	10	Wrap 32	CA[4:0]	XXXXXX1A	1B. 1A, 1D, 1C, 1F, 1E,…. 17, 16, 19, 18, 1B, 1A, 1C, 1B, …
Write	10	Wrap 32	CA[4:0]	XXXXXX1A	1B. 1A, 1D, 1C, 1F, 1E,…. 17, 16, 19, 18, 1B, 1A, 1C, 1B, …
Read	11	Wrap 16	CA[3:0]	XXXXXX0A	0B. 0A, 0D, 0C, 0F, 0E, 01, 00,…. 07, 06, 09, 08, 0B, 0A, …
Write	11	Wrap 16	CA[3:0]	XXXXXX0A	0B. 0A, 0D, 0C, 0F, 0E, 01, 00,…. 07, 06, 09, 08, 0B, 0A, …
Read	XX	Continuous	X	XXXXXX0C	0D, 0C, 0F, 0E, 11, 10, 13, 12, 15, 14, 17, 16, 19. 18, …
Write	XX	Continuous	X	XXXXXX0C	0D, 0C, 0F, 0E, 11, 10, 13, 12, 15, 14, 17, 16, 19. 18, …

Notes: When Continuous burst type is operated on burst operations, Memory access address will increase continuously regardless of Burst Wrap Length code.

6.2.2 INITIAL LATENCY (CR [3])

Initial Latency for Fixed Latency setting (CR [3] = 1) is always 2LC.

Table 6.5 Fixed Latency (CR[3] = 1)

Latency code CR[7:4]	Fixed mode Initial Latency Counter (2LC)	Maximum Operating Frequency	
		1.8V	3.0V
0000	6 clocks	83Mhz	83Mhz
0001	8 clocks	100Mhz	100Mhz
0010	**10 clocks (default at 3V)**	166Mhz	**133Mhz**
0011	12 clocks	166MHz	166MHz
0100	14 clocks	200MHz	166MHz
0101	**16 clocks (default at 1.8V)**	**200Mhz**	166MHz
0100 - 1111	Reserved	NA	

Notes: Default setting for 1.8V device is “0101”, and that for 3.0V device is “0010”.

Table 6.6 Initial Latency Summary Table

Destination	Operating mode	Fixed mode Initial Latency Count
Memory	READ	2LC
	WRITE	**2LC(2)**
Register	READ	**2LC(2)**
	WRITE	0LC

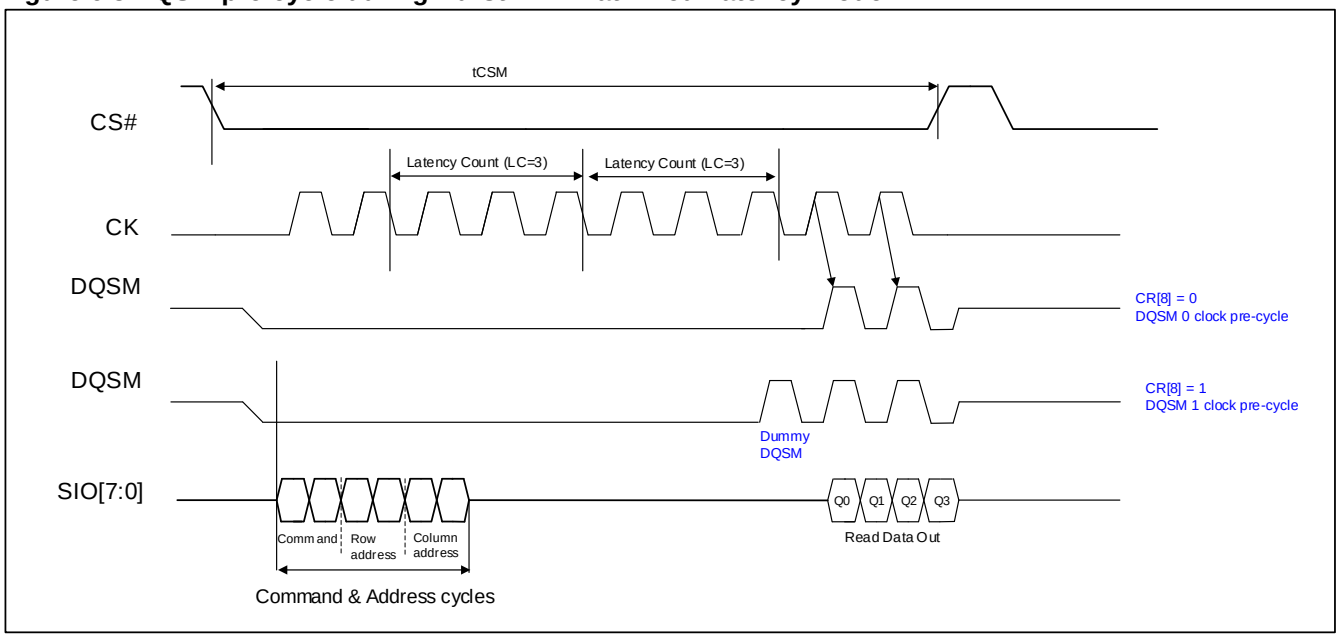
Notes:

1. LC means Latency Counter clocks, which is in Configuration Register Bit [7:4], as defined in *"Table 6.1" and ."Table 6.3"*.

6.2.3 DQSM READ Pre-Cycle (CR [8])

CR [8] defines DQSM Pre-Cycle.

Figure 6.3 DQSM pre-cycle during Burst READ at Fixed Latency mode



Notes:

1. Latency count (LC) is 3 clocks.
2. When Configuration Register bit8 = 0, the Device will output DQSM with valid data cycle.
3. When Configuration Register bit8 = 1, the Device will output dummy DQSM one clock cycle period prior to valid data cycle.
4. The memory drives DQSM during read cycles.

6.2.4 Deep Power Down (CR [15])

512Mb is a DDP device, so Deep Power Down function is not supported.

6.3 DEVICE IDENTIFICATION REGISTER

It is a read only, non-volatile, word register that provides device information The device information fields can be identified as below.

b. Device Type
c. Density
    i. Row address bit count
    ii. Column address bit count
d. Manufacturer

The device is a DDP device of two 256Mb, so each die must be read out individually.

Table 6.7 ID Register

Bits	Function	Settings (Binary)
15 - 13	Device Voltage	000: 1.8V 001: 3V
12 - 8	Row address bit count	00000 : 1 row address ……. 01111 : 16 row address …….. 11111 : 32 row address
7 - 4	Column address bit count	0000 : 1 column address ….. 1001: 10 column address ….. 1111 : 16 column address
3 - 0	Manufacturer	0011 (ISSI)

7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature	-65°C to +150°C
Input Voltage with Respect to Ground on All Pins	-0.5V to V_{CC} + 0.5V
All Output Voltage with Respect to Ground	-0.5V to V_{CC} + 0.5V
V_{CC}	-0.5V to +4.0V
Electrostatic Discharge Voltage (Human Body Model)(2)	-2000V to +2000V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

7.2 OPERATING RANGE

Operating Temperature	Industrial Grade	-40°C to 85°C
	Automotive Grade A1	-40°C to 85°C
	Automotive Grade A2	-40°C to 105°C
V_{CC} Power Supply	IS66/67WVO64M8DALL	1.70V (VMIN) –1.95V (VMAX); 1.8V (Typ)
	IS66/67WVO64M8DBLL	2.7V (VMIN) –3.6V (VMAX); 3.0V (Typ)

7.3 DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Leakage Current 3V Device Reset Signal Only	-	-	±20.0	uA	VIN = VSS to VCC, VCC = VCC max
I_{LI}	Input Leakage Current 1.8V Device Reset Signal Only	-	-	±10.0	uA	VIN = VSS to VCC, VCC = VCC max
I_{CC1}	VCC Active Read Current	-	30	35	mA	CS# = VIL, @200MHz, VCC = 1.9V
			35	40		CS# = VIL, @166MHz, VCC = 3.6V
I_{CC2}	VCC Active Write Current	-	25	30	mA	CS# = VIL, @200MHz, VCC = 1.9V
			30	35		CS# = VIL, @166MHz, VCC = 3.6V
I_{CC4I}	VCC Standby Current for Industrial (-40°C to +85°C)	-	1400	1500	uA	CS#, VCC=VCC max
I_{CC4IP}	VCC Standby Current for Extended (-40°C to +105°C)	-	1400	1800		
I_{CC5}	Reset Current	-	10	20	mA	CS# = VIH, RESET# = VSS +/- 0.3V, VCC = VCC max
I_{CC6I}	Active Clock Stop Current for Industrial (-40°C to +85°C)	-	10	20	mA	CS# = VIL, RESET# = VCC +/- 0.3V, VCC = VCC max
I_{CC6IP}	Active Clock Stop Current for Extended (-40°C to +105°C)	-	10	20		
I_{CC7}	VCC Current during power up	-	-	80	mA	CS#,= H, VCC= VCC max, VCC=VCCQ= 1.95V or 3.6V
V_{IL}(1)	Input Low Voltage	-0.5	-	$0.3V_{CC}$	V	
V_{IH}(1)	Input High Voltage	$0.7V_{CC}$	-	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		-	0.2	V	I_{OL} = 100 µA
V_{OH}	Output High Voltage	V_{CC} - 0.2	-		V	I_{OH} = -100 µA

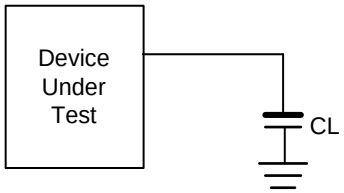
Notes:

1. **Maximum DC voltage on input or I/O pins is VCC + 0.5V. During voltage transitions, input or I/O pins may overshoot VCC by +2.0V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -2.0V for a period of time not to exceed 20ns.**
2. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ).**

7.4 AC MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Max	Units
CL	Output Load Capacitance		20	pF
TR,TF	Input Rise and Fall Times	2		V/ns
VIN	Input Pulse Voltages	0V to V_{CCQ}		V
VREFI	Input Timing Reference Voltages	VCCQ/2		V
VREFO	Output Timing Reference Voltages	VCCQ/2		V

Figure 7.1 Test Setup



7.5 PIN CAPACITANCE (TA = 25°C, VCC=1.8V/ 3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance (CS#, SCLK)	V_{IN} = 0V	6	-	9.0	pF
$C_{IN/OUT}$	Input/Output Capacitance (SIO, DQSM)	$V_{IN/OUT}$ = 0V	6	-	8.0	pF

Note:
1. These parameters are characterized and not 100% tested.

7.6 AC CHARACTERISTICS

7.6.1 Read Timing Parameters (1.8V)

Symbol	Parameter	200MHz		166MHz		Unit
		Min.	Max.	Min.	Max.	
LC	Latency Counter (No Refresh Collision)	7	-	6	-	clock
tRWR	Read-Write Recovery Time	35	-	36	-	ns
tCK	Clock(CLK) Period	5	-	6	-	ns
tCH	Clock High level width	0.45	-	0.45	-	tCKmi
tCL	Clock Low level width	0.45	-	0.45	-	tCKmi
tHP	Clock half period	Min(tCH,tCL)	-	Min(tCH,tCL)	-	ns
tDQSV	CS# Active to DQSM valid	-	12	-	12	ns
tAC	Clock transition to DQ valid	0.9	5.5	1	5.5	ns
tDQSCK	Clock transition to DQSM valid	0.9	5.5	1	5.5	ns
tCSP	CS# High Between READ/WRITE	7	-	7	-	ns
tCSS	CS# Setup to next CLK Rising Edge	3	-	3	-	ns
tCSH	CS# Hold After CLK Falling Edge	2	-	2	-	ns
tIS	Input Setup	0.6	-	0.6	-	ns
tIH	Input Hold	0.6	-	0.6	-	ns
tDQSQ	DQSM-DQ Skew	-	0.4	-	0.45	ns
tQHS	Data Hold Skew factor	-	0.8	-	0.85	ns
tQH	DQ hold time from DQSM	tHP-tQHS	-	tHP-tQHS	-	ns
tLZ	Clock to DQ Low-Z	0	-	0	-	ns
tHZ	CS# Inactive to DQSM and DQ High-Z	-	5	-	6	ns
tCSM	Chip Select Maximum Low Time (~ 85°C)	-	4.0	-	4.0	us
tCSM	Chip Select Maximum Low Time (~ 105°C)	-	1.0	-	1.0	us

7.6.2 Read Timing Parameters (3.0V)

Symbol	Parameter	166MHz		133MHz		Unit
		Min.	Max.	Min.	Max.	
LC	Latency Counter (No Refresh Collision)	6	-	5	-	clock
tRWR	Read-Write Recovery Time	36	-	37.5	-	ns
tCK	Clock(CLK) Period	6	-	7.5	-	ns
tCH	Clock High level width	0.45	-	0.45	-	tCKmi
tCL	Clock Low level width	0.45	-	0.45	-	tCKmi
tHP	Clock half period	Min(tCH,tCL)	-	Min(tCH,tCL)	-	ns
tDQSV	CS# Active to DQSM valid	-	12	-	12	ns
tAC	Clock transition to DQ valid	1	7	1	7	ns
tDQSCK	Clock transition to DQSM valid	1	7	1	7	ns
tCSP	CS# High Between READ/WRITE	7	-	7	-	ns
tCSS	CS# Setup to next CLK Rising Edge	3	-	3	-	ns
tCSH	CS# Hold After CLK Falling Edge	2	-	2	-	ns
tIS	Input Setup	0.6	-	0.8	-	ns
tIH	Input Hold	0.6	-	0.8	-	ns
tDQSQ	DQSM-DQ Skew	-	0.7	-	0.75	ns
tQHS	Data Hold Skew factor	-	0.85	-	0.90	ns
tQH	DQ hold time from DQSM	tHP-tQHS	-	tHP-tQHS	-	ns
tLZ	Clock to DQ Low-Z	0	-	0	-	ns
tHZ	CS# Inactive to DQSM and DQ High-Z	-	6	-	7	ns
tCSM	Chip Select Maximum Low Time (~ 85°C)	-	4.0	-	4.0	us
tCSM	Chip Select Maximum Low Time (~ 105°C)	-	1.0	-	1.0	us

7.6.3 WRITE Timing Parameters (1.8V)

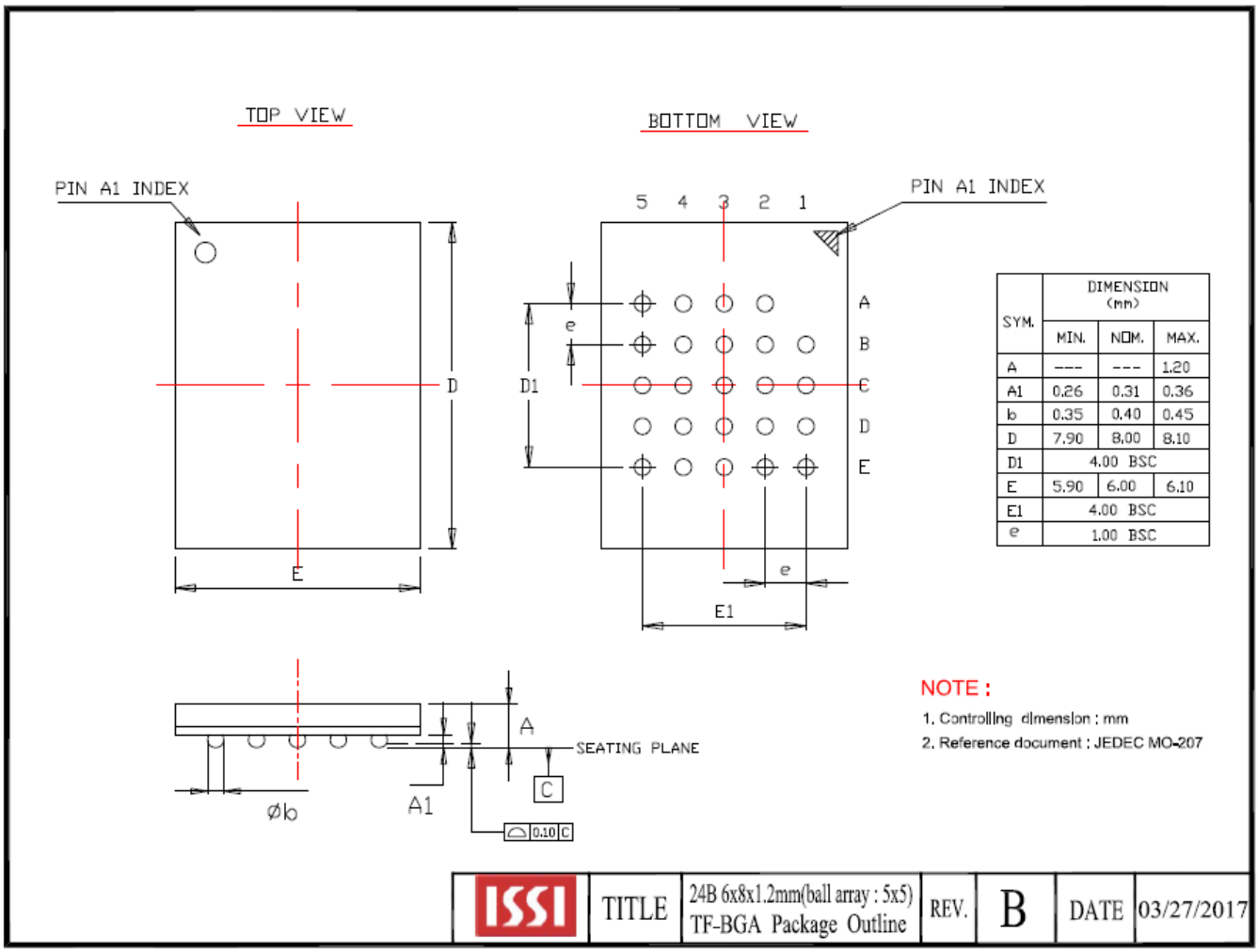
Symbol	Parameter	200MHz		166MHz		Unit
		Min.	Max.	Min.	Max.	
LC	Latency Counter (No Refresh Collision)	7	-	6	-	clock
tRWR	Read-Write Recovery Time	35	-	36	-	ns
tCK	Clock(CLK) Period	5	-	6	-	ns
tCH	Clock High level width	0.45	-	0.45	-	tCKmin
tCL	Clock Low level width	0.45	-	0.45	-	tCKmin
tHP	Clock half period	Min(tCH,tCL)	-	Min(tCH,tCL)	-	ns
tDQSV	CS# Active to DQSM valid	-	12	-	12	ns
tDQSCK	Clock transition to DQSM valid	0.9	5.5	1	5.5	ns
tCSP	CS# High Between READ/WRITE	7	-	7	-	ns
tCSS	CS# Setup to next CLK Rising Edge	3	-	3	-	ns
tCSH	CS# Hold After CLK Falling Edge	2	-	2	-	ns
tIS	Input Setup	0.6	-	0.6	-	ns
tIH	Input Hold	0.6	-	0.6	-	ns
tDMV	Data Mask Valid (DQSM setup to end of initial latency)	0	-	0	-	ns
tCSM	Chip Select Maximum Low Time (~ 85°C)	-	4.0	-	4.0	us
tCSM	Chip Select Maximum Low Time (~ 105°C)	-	1.0	-	1.0	us

7.6.4 WRITE Timing Parameters (3.0V)

Symbol	Parameter	166MHz		133MHz		Unit
		Min.	Max.	Min.	Max.	
LC	Latency Counter (No Refresh Collision)	6	-	5	-	clock
tRWR	Read-Write Recovery Time	36	-	37.5	-	ns
tCK	Clock(CLK) Period	6	-	5	-	ns
tCH	Clock High level width	0.45	-	0.45	-	tCKmin
tCL	Clock Low level width	0.45	-	0.45	-	tCKmin
tHP	Clock half period	Min(tCH,tCL)	-	Min(tCH,tCL)	-	ns
tDQSV	CS# Active to DQSM valid	-	12	-	12	ns
tDQSCK	Clock transition to DQSM valid	1	7	1	7	ns
tCSP	CS# High Between READ/WRITE	7	-	7	-	ns
tCSS	CS# Setup to next CLK Rising Edge	3	-	3	-	ns
tCSH	CS# Hold After CLK Falling Edge	2	-	2	-	ns
tIS	Input Setup	0.6	-	0.8	-	ns
tIH	Input Hold	0.6	-	0.8	-	ns
tDMV	Data Mask Valid (DQSM setup to end of initial latency)	0	-	0	-	ns
tCSM	Chip Select Maximum Low Time (~ 85°C)	-	4.0	-	4.0	us
tCSM	Chip Select Maximum Low Time (~ 105°C)	-	1.0	-	1.0	us

8. PACKAGE TYPE INFORMATION

8.1 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 BALL ARRAY (B)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

9. ORDERING INFORMATION – Valid Part Numbers

IS66 WVO 64M8 D ALL - 200 B L I

TEMPERATURE RANGE
I = Extended (-40°C to +85°C)
A1 = Automotive Grade (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = Green Package **(**RoHS Compliant, Halogen-free) and TSCA Compliant

PACKAGE Type (1)
B = 24-ball TFBGA 6x8mm 5x5 ball array

Maximum Frequency
200 = 200MHz
166 = 166MHz
133 = 133MHz

VDD
ALL = 1.8V
BLL = 3.0V

Die Revision
D = die rev D

Density/Org.
64M8 = 64Mbx8=512Mb

PSRAM Product Type.
WVO = OctalRAM

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
66 = PSRAM
67 = PSRAM for Automotive

Industrial Temperature Range (-40°C to +85°C)

Config.	Voltage	Max. Frequency (MHz)	Order Part Number(1)	Package
64Mbx8	1.8V	200	IS66WVO64M8DALL-200BLI	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS66WVO64M8DALL-166BLI	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	166	IS66WVO64M8DBLL-166BLI	24-ball TFBGA 6x8mm 5x5 ball array
		133	IS66WVO64M8DBLL-133BLI	24-ball TFBGA 6x8mm 5x5 ball array

Automotive A1 Temperature Range (-40°C to +85°C)

Config.	Voltage	Max. Frequency (MHz)	Order Part Number(1)	Package
64Mbx8	1.8V	200	IS67WVO64M8DALL-200BLA1	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS67WVO64M8DALL-166BLA1	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	166	IS67WVO64M8DBLL-166BLA1	24-ball TFBGA 6x8mm 5x5 ball array
		133	IS67WVO64M8DBLL-133BLA1	24-ball TFBGA 6x8mm 5x5 ball array

Automotive A2 Temperature Range (-40°C to +105°C)

Config.	Voltage	Max. Frequency (MHz)	Order Part Number(1)	Package
64Mbx8	1.8V	200	IS67WVO64M8DALL-200BLA2	24-ball TFBGA 6x8mm 5x5 ball array
		166	IS67WVO64M8DALL-166BLA2	24-ball TFBGA 6x8mm 5x5 ball array
	3.0V	166	IS67WVO64M8DBLL-166BLA2	24-ball TFBGA 6x8mm 5x5 ball array
		133	IS67WVO64M8DBLL-133BLA2	24-ball TFBGA 6x8mm 5x5 ball array