



IS66WVQ2M4EDALL/BLL

IS67WVQ2M4EDALL/BLL

8Mb QUADRAM with On Chip ECC
1.8V/3.0V SERIAL PSRAM MEMORY WITH 166MHZ QUAD DDR
(x4 xSPI INTERFACE) PROTOCOL

DATA SHEET

8Mb QUADRAM with On Chip ECC

SERIAL PSRAM MEMORY WITH 166MHz QUAD DDR (x4 xSPI) Interface

FEATURES

• Industry Standard Serial Interface

- Quad DDR (x4 xSPI) Interface:
Command (1 byte) =SDR
Address (2-byte) & Data = DDR
- Low Signal Counts :7 Signal pins (CS#, SCLK, DQSM, SIO0~SIO3)

• High Performance

- On chip ECC (chunk size = 4 bit):
1-bit correction and 2-bit detection
- Double Data Rate (DDR) Operation:
166MHz (166MB/s) at 1.8V VCC ⁽¹⁾
133MHz (133MB/s) at 3.0V VCC
- Source Synchronous Output signal during Read Operation (DQSM)
- Data Mask during Write Operation (DQSM)
- Configurable Latency for Read/Write Operation
- Supports Variable Latency mode and Fixed Latency mode
- Configurable Drive Strength
- Supports Wrapped Burst mode and Continuous mode
- Supports Deep Power Down mode
- Hidden Refresh

• Burst Operation

- Configurable Wrapped Burst Length :
16, 32, 64, and 128
- Continuous Operation:
 - Continues Read operation until the end of array address (No Wrapped)
 - Continues Write operation even after the end of array address (Wrapped to first address)

• Low Power Consumption

- Single 1.7V to 1.95V Voltage Supply
- Single 2.7V to 3.6V Voltage Supply
- 18 mA Operating at 166MHz (1.8V, max.)

• Hardware Features

- **SCLK Input:** Serial clock input
- **SIO0 – SIO3:**
Serial Data Input or Serial Data Output
- **DQSM:**
 - Output during command, address transactions as Refresh Collision Indicator
 - Output during read data transactions as Read Data Strobe
 - Input during write data transactions as Write Data Mask
- **RESET#:** Hardware Reset pin

• Temperature Grades

- Industrial: -40°C to +85°C
- Auto (A2) Grade: -40°C to +105°C

• Industry Standard PACKAGE

- B = 24-ball TFBGA 6x8mm 5x5 Array
- KGD (Call Factory)

GENERAL DESCRIPTION

The IS66/67WVQ2M4EDALL/BLL are integrated memory device containing 8Mb Pseudo Static Random Access Memory, using a self-refresh DRAM array organized as 2M words by 4 bits.

The device supports Quad DDR interface, which is compatible with JEDEC standard x4 xSPI Flash.

The device supports Very Low Signal Count (7 signal pins; SCLK, CS#, DQSM, and 4 SIOs) + optional ERR, Hidden Refresh Operation, and Automotive temperature (A2, -40°C to +105°C) operation.

Due to DDR operation, minimum transferred data size is a byte (8 bits) through 4 SIO pins.

PERFORMANCE SUMMARY

| Read / Write Operation | | |
|------------------------|------|--------------------|
| Package | VCC | Maximum Clock Rate |
| 24-ball BGA | 1.8V | 166MHz |
| | 3.0V | 133MHz |

| Maximum Current Consumption | | |
|---|------|--------|
| Burst Read or Write (Continuous Burst at 166MHz, 1.8V) | | 18 mA |
| Power On Reset | | 20 mA |
| Standby (CS# = High, 105°C) | 3V | 300 uA |
| | 1.8V | 300 uA |
| Deep Power Down (CS# = High, 105°C) | 3V | 50 uA |
| | 1.8V | 30 uA |

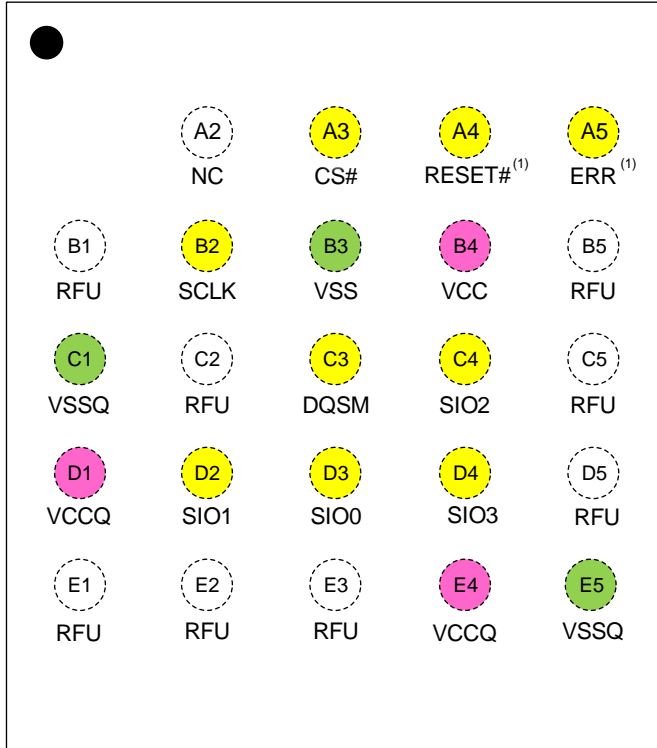
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1. PIN CONFIGURATION

24-ball TFBGA (5x5 ball array)

Top View, Balls Facing Down



Note:

1. RESET# and ERR pins can be left floating when not used.

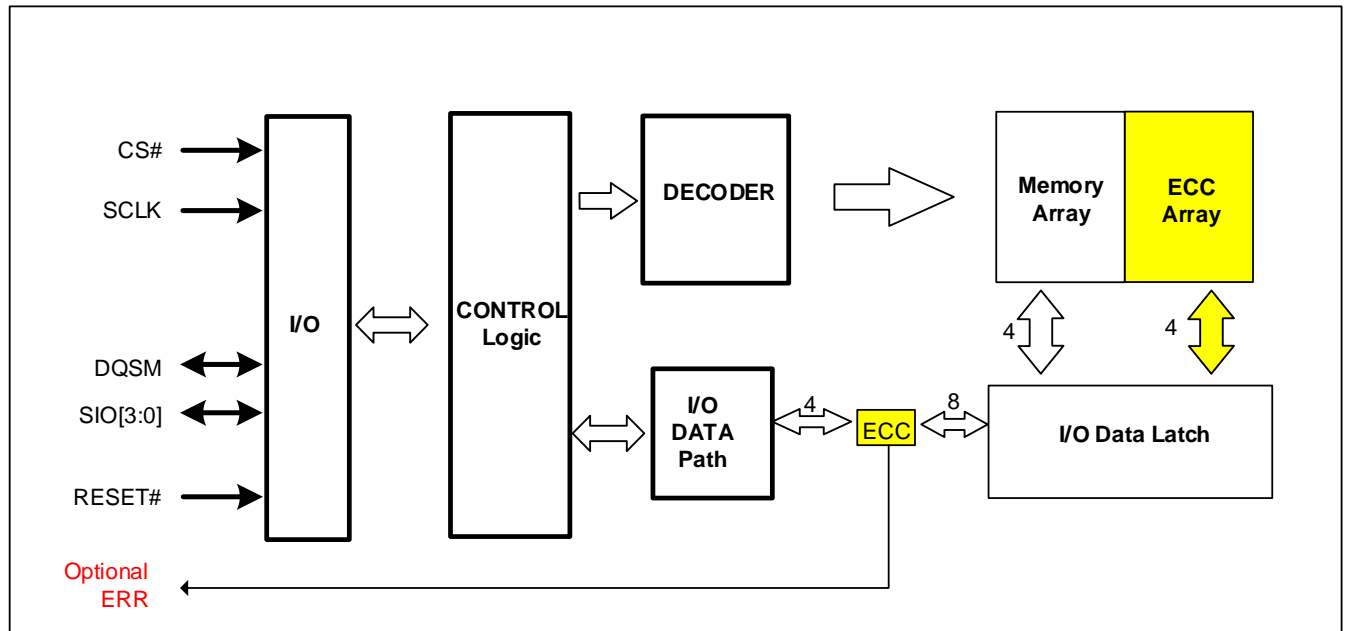
2. PIN DESCRIPTIONS

| SYMBOL | TYPE | DESCRIPTION |
|-----------------------|--------------|---|
| CS# | INPUT | Chip Select: |
| DQSM | INPUT/OUTPUT | Refresh Collision Indicator ⁽²⁾, Data Strobe Signal in Read operation, and Write Data Mask in Write operation: |
| RESET# ⁽¹⁾ | INPUT | RESET#: The RESET# pin is a hardware RESET signal. When RESET# is driven High, the memory is in the normal operating mode. When RESET# is driven Low, the memory enters reset mode and output is High-Z. |
| SIO0-SIO3 | INPUT | Serial Data Input & Output pins. |
| SCLK | INPUT | Serial Data Clock: Synchronized Clock for input and output timing operations. |
| ERR | OUTPUT | Error Indicator: Indicates ECC Event Occurrence. Optional output signal, so leave it as floating is fine. |
| VCC | POWER | Power Supply |
| VCCQ | POWER | IO Power Supply |
| VSS | GROUND | Ground |
| VSSQ | GROUND | IO Ground |
| RFU | Reserved | RFU: Reserved for future use: May or may not be connected internally. |

Notes:

1. RESET# pin has an internal pull-up.
2. Contact ISSI MKT for DQSM without Refresh Collision Indicator

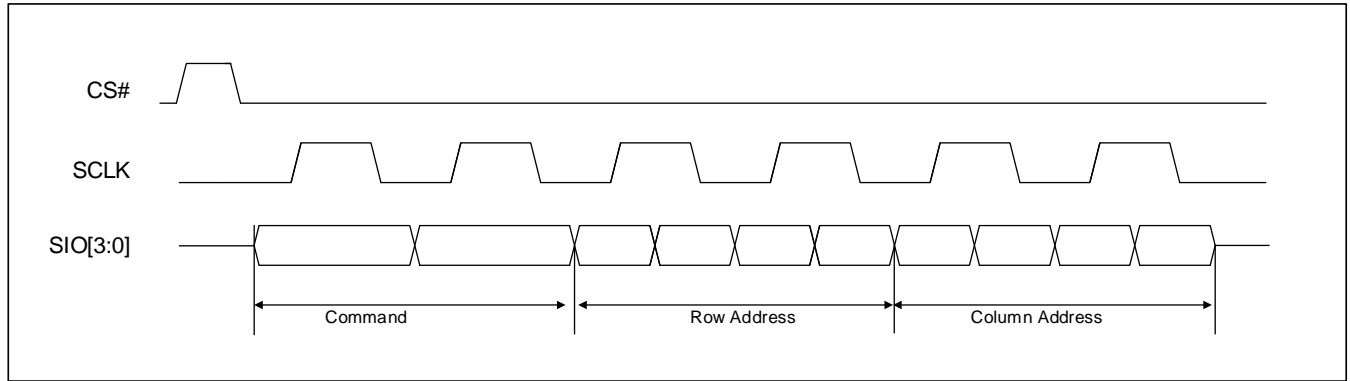
3. BLOCK DIAGRAM



4. COMMAND AND ADDRESS ASSIGNMENTS

The device is serial interface, so all command and address inputs are transferred through SIO pins.

Figure 4.1 Command and Address Cycles



Notes:

1. The figure shows the initial six clock cycles of input operations.
2. Command and Address information is “center aligned” with the clock during both Read and Write operations.

Table 4.1 Command / Address bit assignment

| Clock | 1 st clock | 2 nd clock | 3 rd clock | 4 th clock | 5 th clock | 6 th clock | | | | |
|----------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|----------|-----|----------|----------|
| Function | Command (8-bit) | | Row address | | Column address | | | | | |
| SIO[3] | Command | | Reserved | RA11 | RA7 | RA3 | Reserved | CA6 | CA2 | Reserved |
| SIO[2] | | | Reserved | RA10 | RA6 | RA2 | Reserved | CA5 | CA1 | Reserved |
| SIO[1] | | | Reserved | RA9 | RA5 | RA1 | Reserved | CA4 | CA0 | Reserved |
| SIO[0] | | | RA12 | RA8 | RA4 | RA0 | Reserved | CA3 | Reserved | Reserved |

Notes:

1. The 16Mb QUADRAM address assignments:
 - Row Address 12 ~ 0: 8K (13 bits), Column Address 6 ~ 0: 128 (7 bits), 8Mb density = 8K X 128 (bytes)
2. Data is always transferred in full byte increment (byte granularity -8 bits-transfer).

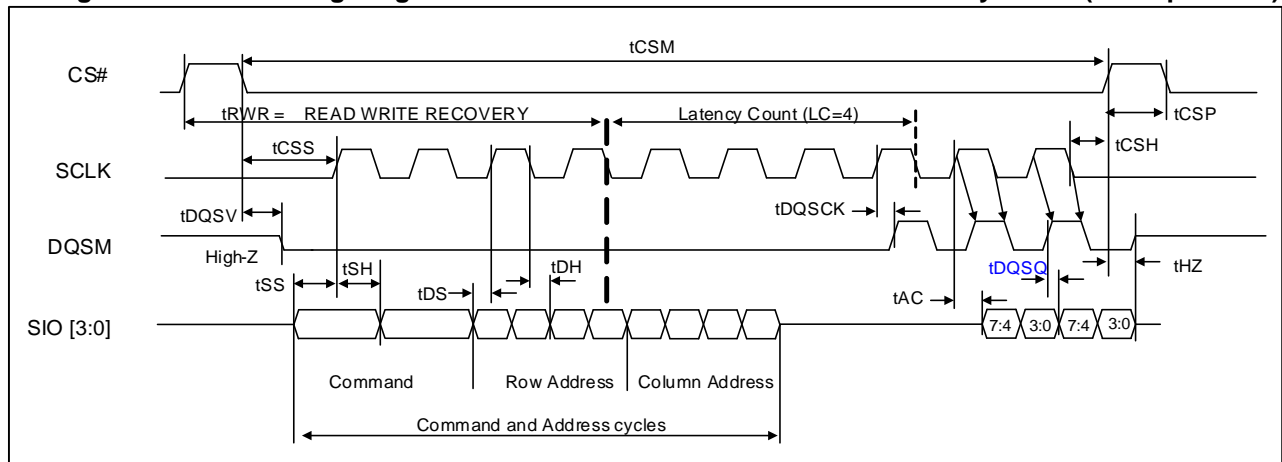
Table 4.2 Command / Address bit assignment

| Command | Clock 1, 2 | | Clock 3, 4 | | Clock 5, 6 | |
|-------------------------------------|---------------|----|-------------------|-----|---|------------|
| | Command (SDR) | | Row address (DDR) | | Column address (DDR) | |
| Memory READ with continuous burst | Ah | 0h | RA[12:0] | | CA[6:0] | |
| Memory READ with wrapped burst | 8h | 0h | RA[12:0] | | CA[6:0] | |
| Memory WRITE with continuous burst | 2h | 0h | RA[12:0] | | CA[6:0] | |
| Memory WRITE with wrapped burst | 0h | 0h | RA[12:0] | | CA[6:0] | |
| Identification Register (read only) | Ch or Eh | 0h | 00h | 00h | 00h | 00h |
| Configuration Register READ | Ch or Eh | 0h | 00h | 04h | 00h | 00h |
| Configuration Register WRITE | 6h | 0h | 00h | 04h | 00h | 00h |
| ECC Register READ | Ch or Eh | 0h | 00h | 04h | 00h | 03h |
| ECC Register WRITE | 6h | 0h | 00h | 04h | 00h | 03h |
| Preamble Bit Pattern READ | Fh | 0h | Don't care | | CA[6:1] Don't care CA[0] Pattern Selection | |

5. Memory READ/WRITE OPERATIONS

5.1 MEMORY READ OPERATIONS

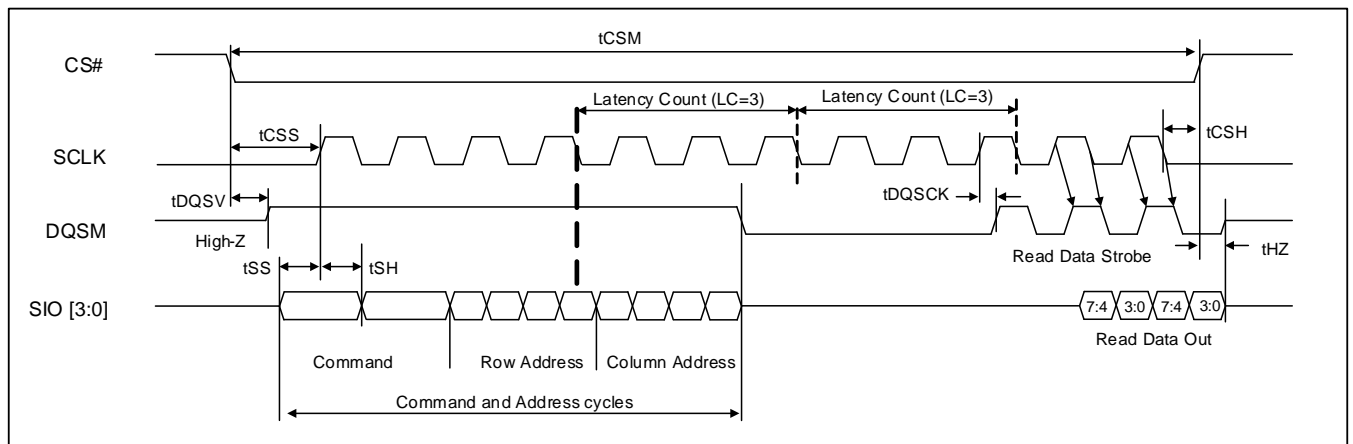
Figure 5.1 Read Timing Diagram - No Refresh Collision at Variable Latency READ (1LC operation)



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 4 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with no refresh collision access**.
4. Read access (LC) starts once RA [3:0] (falling edge of 4th clock) is captured.
5. The memory drives DQSM during read cycles.
6. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the device.

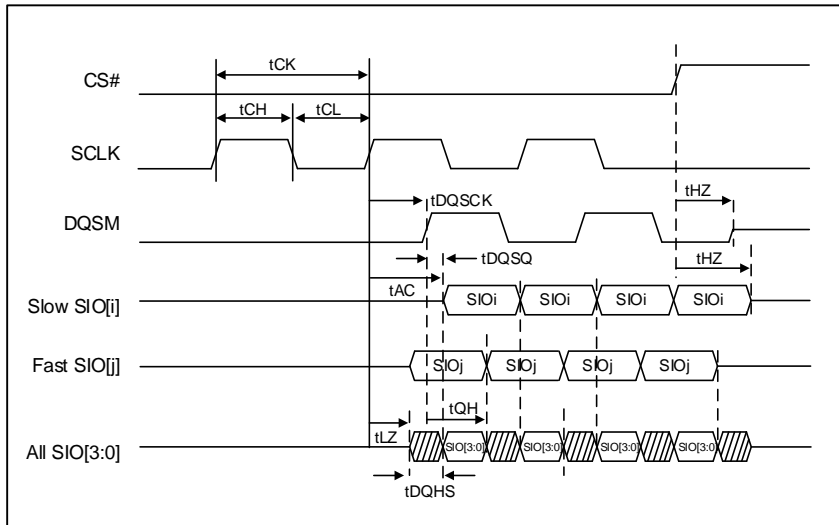
Figure 5.2 Read Timing Diagram - Refresh Collision at Variable-Latency READ (2LC operation)



Notes:

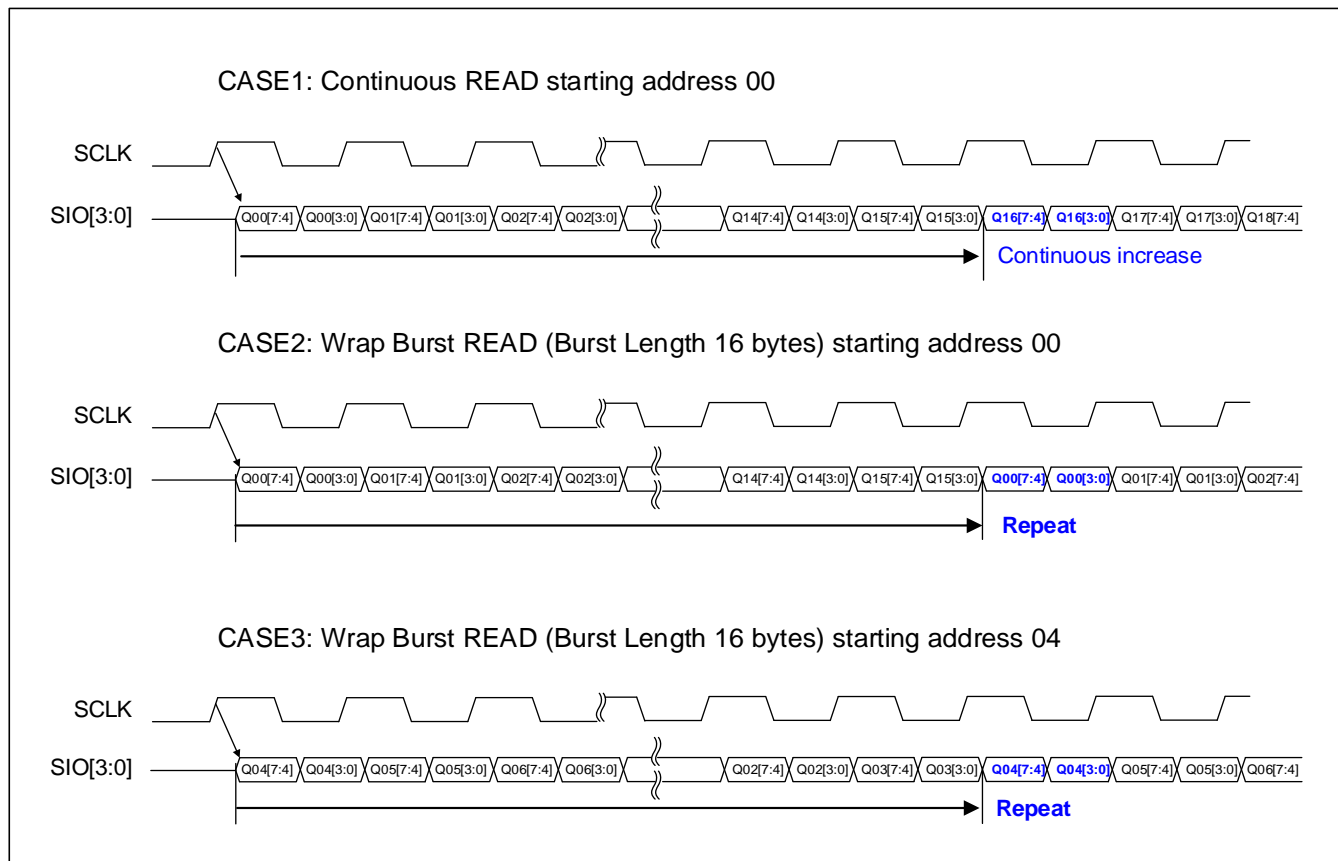
1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with refresh collision or fixed-latency access (2LC operation)**.
4. In this Read there is a 2 Latency Count (2LC) for read access.
5. Read access (LC) starts once RA [3:0] is captured.
6. The memory drives DQSM during read cycles.
7. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the device.
8. **Fixed initial READ access latency outputs the first data at a consistent time regardless of worst-case refresh collisions.**

Figure 5.3 Data Valid Timing



Notes:

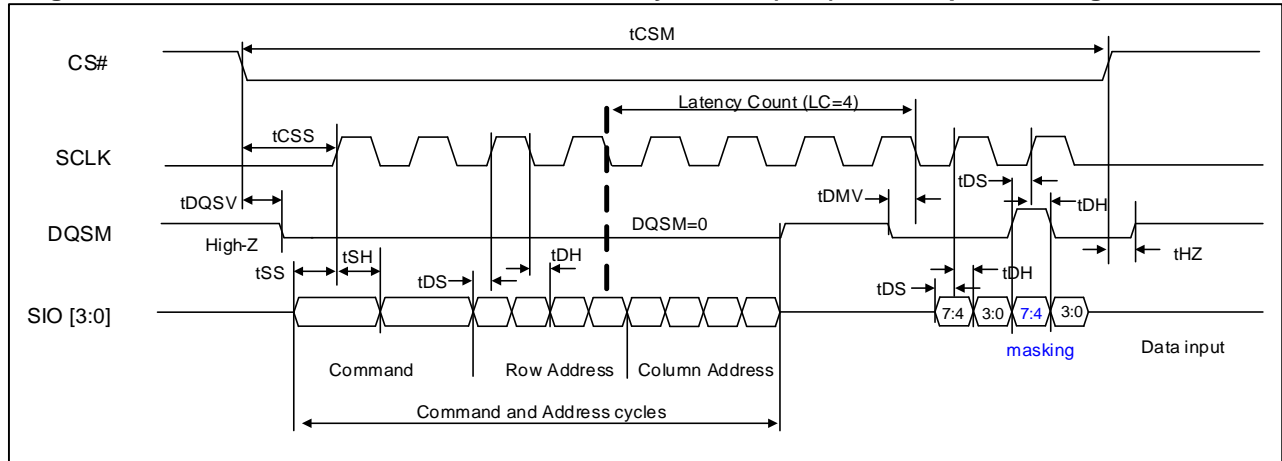
1. Burst READ data valid timing in detail.
2. t_{AC} defines CLK transition to DQ Valid.
3. t_{DQSK} defines CLK transition to DQSM Valid.
4. t_{DQSQ} defines DQSM-DQ skew.
5. t_{QHS} defines Data Hold skew factor.
6. t_{QH} defines DQ hold time from DQSM.

Figure 5.4 READ Burst Wrap

Notes:

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Read operation can be ended at any time by bringing CS# High.
3. Continues Read operation until last address. Continuing beyond last address, undefined data will be available.

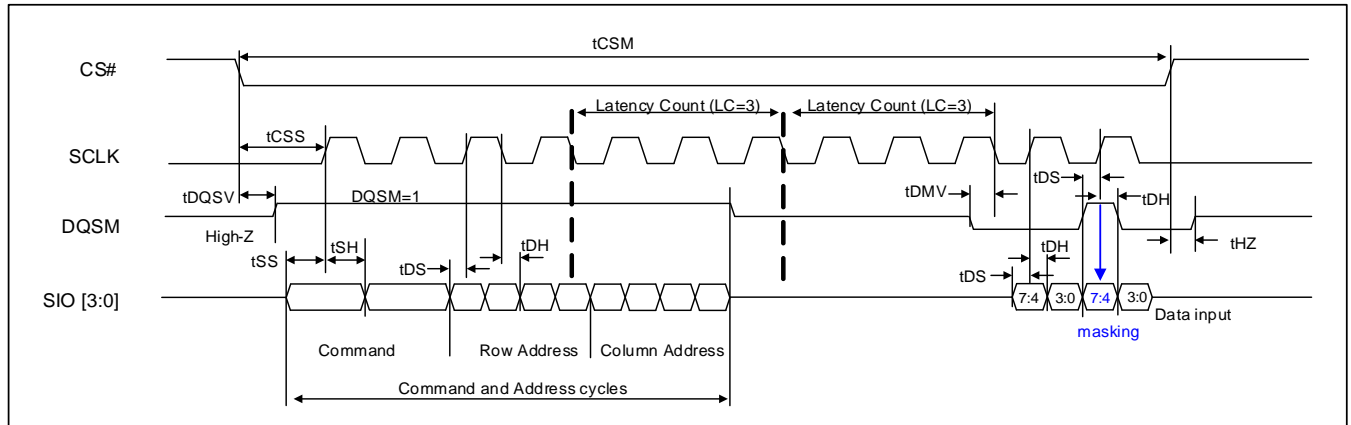
5.2 WRITE OPERATIONS

Figure 5.5 No Refresh Collision at Variable Latency WRITE (1LC) / Data Input Masking



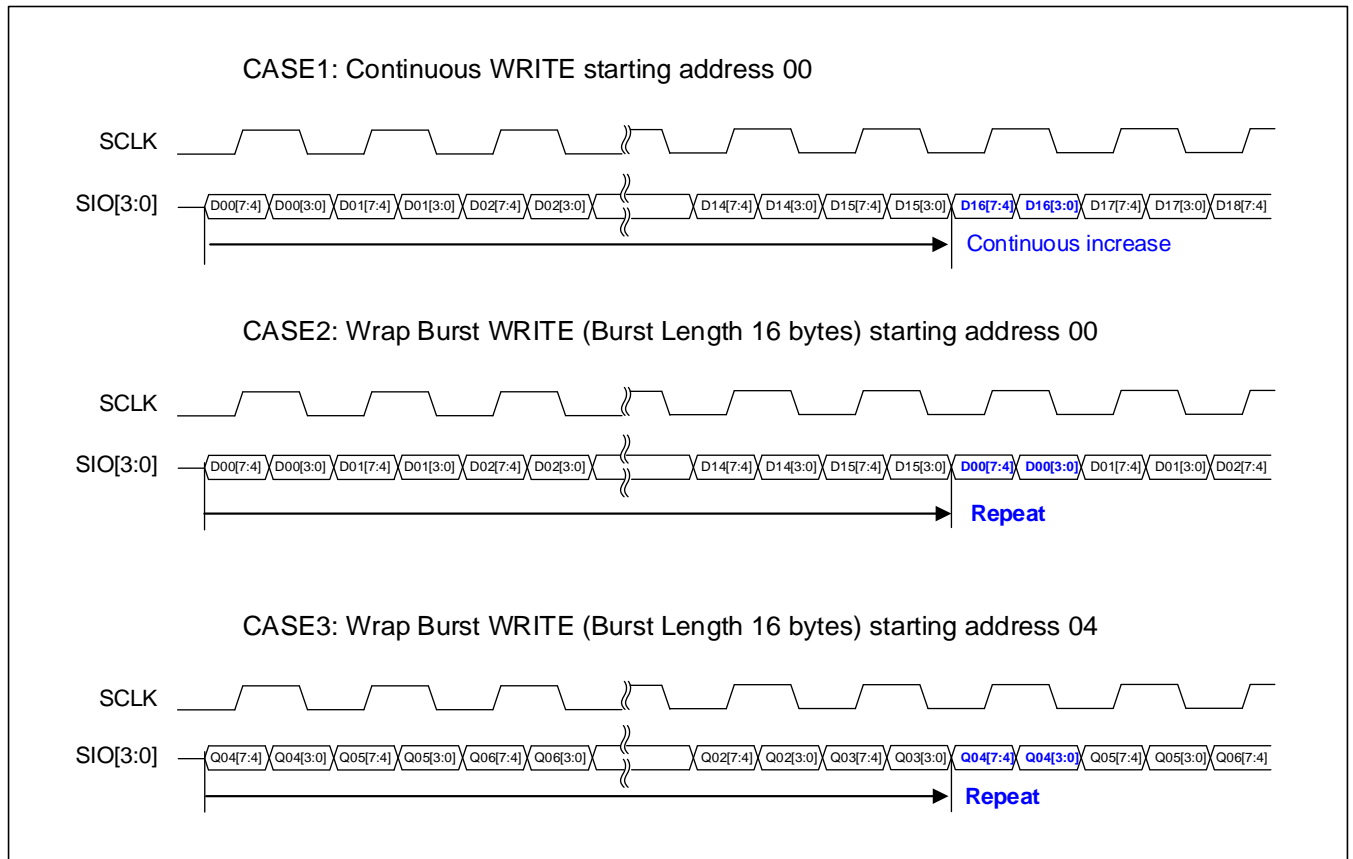
Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 4 clocks.
3. Diagram in the figure above is representative of **variable latency with no refresh collision access**.
4. Write access (LC) starts once RA [3:0] is captured.
5. The memory drives DQSM "Low" during command address cycles and DQSM goes to "Hi-Z" after command address cycles.
6. The system memory controller must drive DQSM to a valid Low before the end of initial latency (t_{DMV}) to provide a data mask preamble time. This can be done during the last cycle of LC cycle.
7. During Write data input, data is center aligned with the clock.
8. During Write data input, DQSM indicates whether each data byte is masked with DQSM High or not masked with DQSM Low.
9. Data inputs [7:4] of second byte are masked.

Figure 5.6 Refresh Collision at Variable Latency WRITE (2LC) / Data Input Masking

Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks.
3. Diagram in the figure above is representative of **variable latency with refresh collision or fixed-latency access. (2LC operation)**
4. **In this Write there is a latency count (2LC) for WRITE operation**
5. Write access (LC) starts once RA [3:0] is captured.
6. The memory drives DQSM High during command address cycles and DQSM goes to "Hi-Z" after command address cycles.
7. The system memory controller must drive DQSM to a valid Low before the end of initial latency (t_{DMV}) to provide a data mask preamble time. This can be done during the last cycle of LC cycle.
8. During Write data input, data is center aligned with the clock.
9. During Write data input, DQSM indicates whether each half byte (4-bit) is masked with DQSM High or not masked with DQSM Low.
10. Data inputs [7:4] of second byte are masked.

Figure 5.7 WRITE Burst Wrap



Notes:

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Write operation can be ended at any time by bringing CS# High.
3. When continuous burst write reaches the last address in the memory array, continuing the burst will write to the beginning of the address.

5.3 PREAMBLE BIT DATA PATTERN READ OPERATION

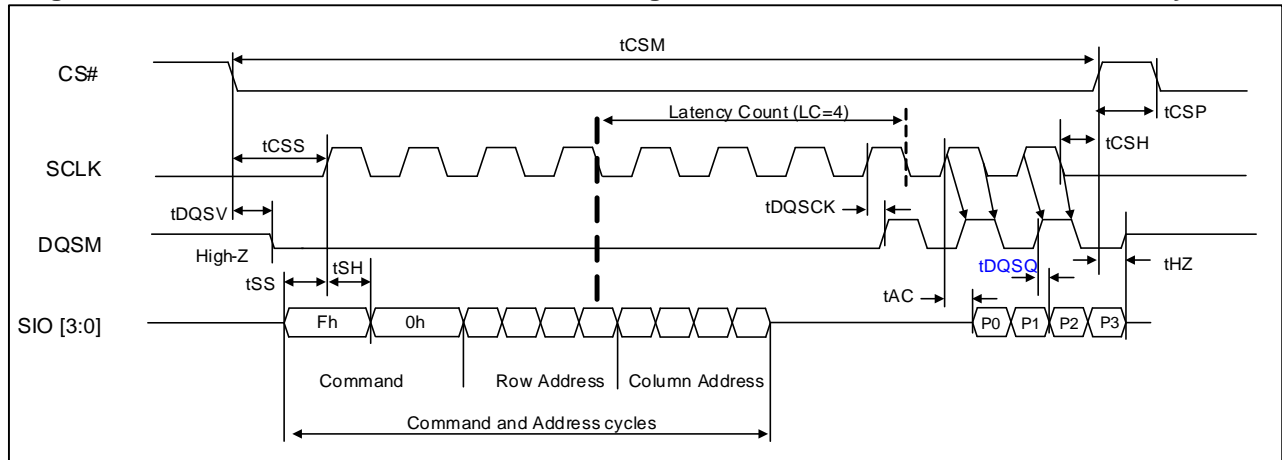
The Preamble Bit Data Pattern READ Operation can improve data capture reliability while the QUADRAM is running in high frequency, while supporting the System/Memory Controller to determine the data output valid windows more easily.

The Preamble Bit is designed as a 16-bits data pattern, it can be output by Preamble Bit READ Command (F0h + 00h). The Row Address and Column Address are “don’t care”, except Column Address CA0 is used for selecting the pattern.

After Preamble Bit READ Command (F0h).and addresses cycles, a fixed 16-bits data pattern will output after initial latency cycles on all 4-SIO pins, according to A0 setting in Column Address. Refer to "Table 5.1. Preamble Bit Data Pattern SIO assignments".

The Latency Count values are defined in configuration register CR [7-4] which is the same as Read timing diagram.

Figure 5.8 Preamble Bit Data Pattern READ Timing, No Refresh Collision at Variable Latency



Notes:

1. Latency Count (LC) = 4 clocks, CR[8]=1 (DQSM 1 clock pre-cycle before Valid READ Data)
2. The memory drives DQSM during the entire Data Learning Pattern Read.
3. The required latency count is device and clock frequency dependent.
4. Column address A0 is used for pattern selection, and Row address RA [12:0] and Column address CA [6:1] are don't care.

Table 5.1 Preamble Bit Data Pattern SIO assignments

| Column Address A0 | All SIOs (except SIO3) | SIO3 |
|-------------------|------------------------|---------------------|
| A0=0 | 0011 0100 1001 1010 | 0011 0101 0001 0100 |
| A0=1 | 0101 0101 0101 0101 | 0101 0101 0101 0101 |

5.4 RESET OPERATION

Figure 5.9 RESET Timing

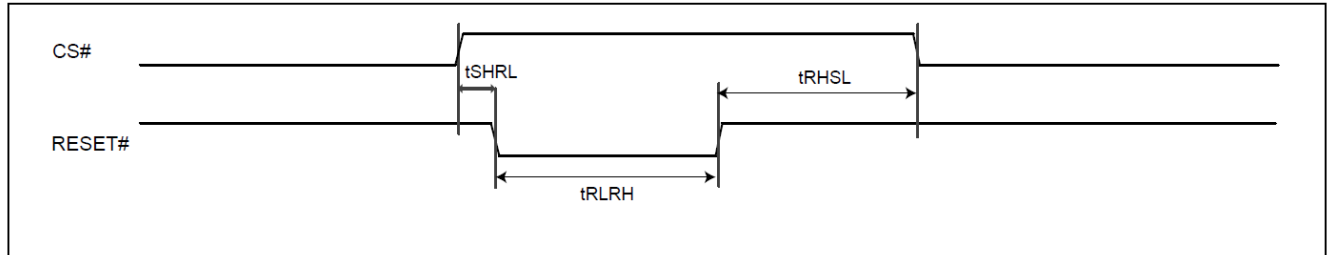
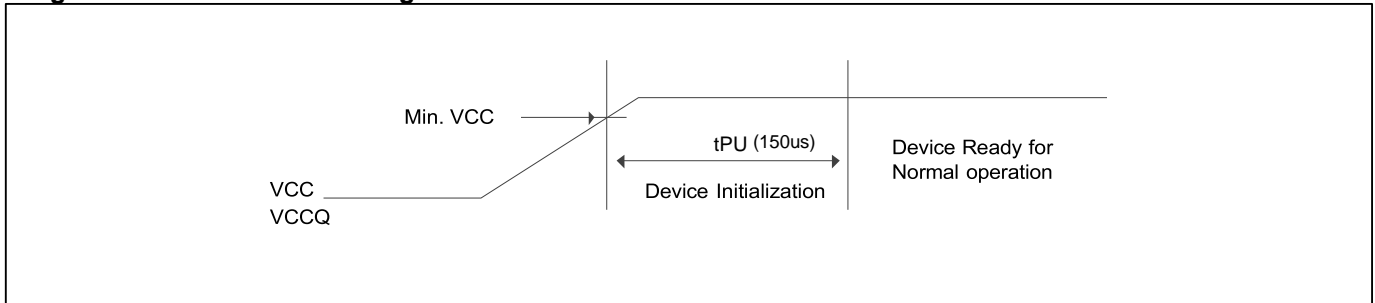


Table 5.2 RESET Timing Parameters

| Parameter | Description | Min | Max | Unit |
|------------|----------------------------|-----|-----|------|
| t_{SHRL} | RESET# Low after CS# High | 15 | - | ns |
| t_{RLRH} | RESET# Low Pulse width | 10 | - | us |
| t_{RHSL} | RESET# High before CS# Low | 10 | - | us |

5.5 POWER-UP INITIALIZATION

Figure 5.10 POWER-UP Timing

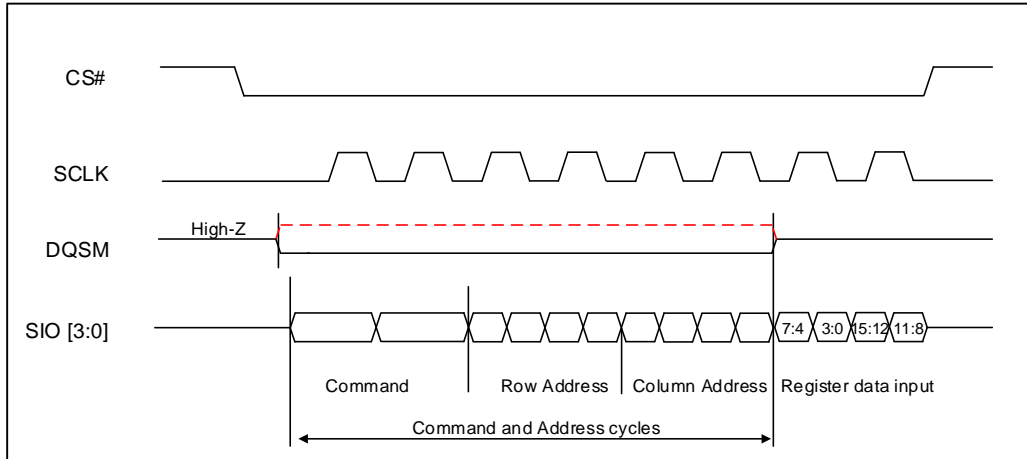


6. REGISTER

The device has 16 bit Configuration Register and ID Register, and they can be accessed by Register Read or Write command.

6.1 REGISTER READ/WRITE OPERATION

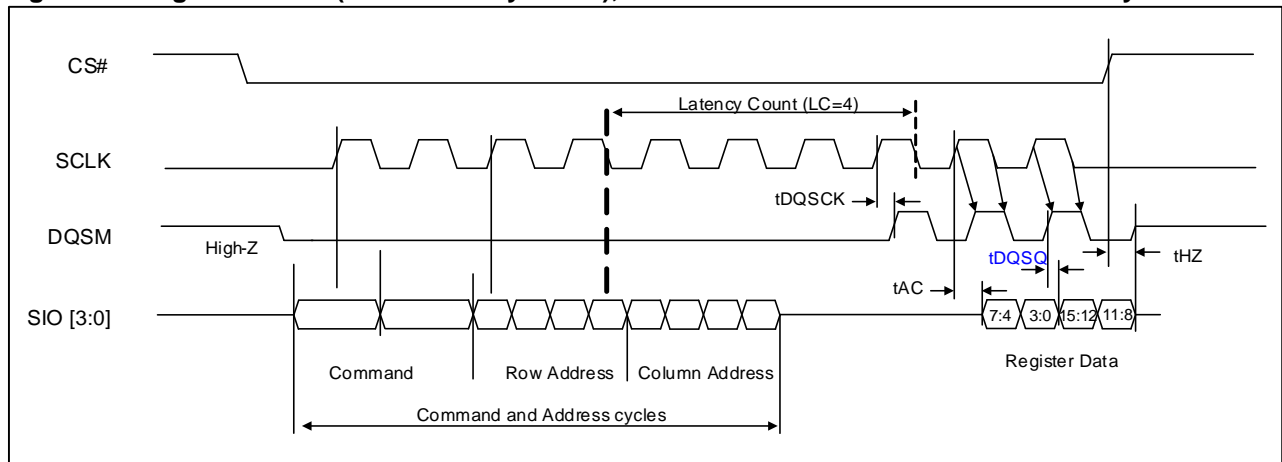
Figure 6.1 Register WRITE



Notes:

1. The device drives DQSM “Low or High for Refresh indication” during command address cycles, which must be ignored by host. DQSM goes to “Hi-Z” after command address cycles.
2. The register value is always provided immediately after the Command Address cycles (0 cycle latency)
3. The DQSM signal keep Hi-Z during register data-input cycles. DQSM will be ignored by host during entire register write operation.
4. **Least Significant Byte first ([7:0]), and Most Significant Byte ([15:8]) later.**

Figure 6.2 Register READ (Initial Latency = 1LC), No Refresh Collision at Variable Latency



Notes:

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 4 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with no refresh collision access**.
4. Read access (LC) starts once RA [3:0] is captured (falling edge of 4th Row address clock)
5. The memory drives DQSM during read cycles.
6. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the device.

6.2 CONFIGURATION REGISTER

The Configuration Register is able to change the defaulted status of the device. The device will be configured after the CR bit is set.

Table 6.1 Configuration Register

| | Bit | Function | Settings (Binary) |
|------------------------|-------|-----------------------------|--|
| Most Significant Byte | 15 | Deep Power Down Enable | 1- Normal operation (default) 0- Writing 0 to CR [15] causes the device to enter Deep Power Down. |
| | 14-12 | ODS (Output Drive Strength) | Refer to " Table 6.2. Output Driver Strength Table " |
| | 11-9 | Reserved | Set to 000b |
| | 8 | DQSM READ Pre-cycle | 1 - 1 clock 0 - 0 clock (default) |
| Least Significant Byte | 7-4 | Latency counter | Refer to " Table 6.3. Latency counter Table " |
| | 3 | Initial Access Latency | 0 - Variable Latency (default) 1 - Fixed Latency |
| | 2 | Reserved | Set to 0b |
| | 1-0 | Burst Length | 00- 128 bytes 01- 64 bytes 10- 32 bytes (default) 11- 16 bytes |

Table 6.2 Output Driver Strength Table

| CR[14] | CR[13] | CR[12] | Description |
|--------|--------|--------|--------------------------|
| 0 | 0 | 0 | 146 Ohms |
| 0 | 0 | 1 | 76 Ohms |
| 0 | 1 | 0 | 52 Ohms |
| 0 | 1 | 1 | 41 Ohms |
| 1 | 0 | 0 | 34 Ohms |
| 1 | 0 | 1 | 30 Ohms |
| 1 | 1 | 0 | 26 Ohms |
| 1 | 1 | 1 | 24 Ohms (Default) |

Table 6.3 Latency counter Table

| CR[7:4] | Latency Counter |
|-------------|----------------------------------|
| 0000 | 3 clocks |
| 0001 | 4 clocks |
| 0010 | 5 clocks(default at 3V) |
| 0011 | 6 clocks |
| 0100 | 7 clocks |
| 0101 | 8 clocks(default at 1.8V) |
| 0110~1111 | Reserved |

6.2.1 WRAPPED BURST LENGTH
Table 6.4 Wrapped Burst Sequences

| Command | Configuration Register[1:0] | Burst Type | Wrap Boundary Col. Addr | Start address (Hex) | Address Sequence (Hex):Bytes |
|---------|-----------------------------|------------|-------------------------|---------------------|---|
| Read | 00 | Wrap 128 | CA[6:0] | XXXXXX06 | 06, 07, 08, 09, 7E, 7F , 00, 01, 02, 03, 04, 05, 06, 07, |
| Write | 00 | Wrap 128 | CA[6:0] | XXXXXX06 | 06, 07, 08, 09, 7E, 7F , 00, 01, 02, 03, 04, 05, 06, 07, |
| Read | 01 | Wrap 64 | CA[5:0] | XXXXXX02 | 02, 03, 04, 05, 3E, 3F , 00, 01, 02, 03, 04, 05, 06, 07, |
| Write | 01 | Wrap 64 | CA[5:0] | XXXXXX02 | 02, 03, 04, 05, 3E, 3F , 00, 01, 02, 03, 04, 05, 06, 07, |
| Read | 10 | Wrap 32 | CA[4:0] | XXXXXX1A | 1A, 1B, 1C, 1D, 1E, 1F , 00, 01, 0E, 0F, 10, 11, 12, |
| Write | 10 | Wrap 32 | CA[4:0] | XXXXXX1A | 1A, 1B, 1C, 1D, 1E, 1F , 00, 01, 0E, 0F, 10, 11, 12, |
| Read | 11 | Wrap 16 | CA[3:0] | XXXXXX0A | 0A, 0B, 0C, 0D, 0E, 0F , 00, 01, 08, 09, 0A, 0B, 0C, |
| Write | 11 | Wrap 16 | CA[3:0] | XXXXXX0A | 0A, 0B, 0C, 0D, 0E, 0F , 00, 01, 08, 09, 0A, 0B, 0C, |
| Read | XX | Continuous | X | XXXXXX0C | 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, |
| Write | XX | Continuous | X | XXXXXX0C | 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, |

Notes: When Continuous burst type is operated on burst operations, Memory access address will increase continuously regardless of Burst Wrap Length code.

6.2.2 INITIAL LATENCY (CR [3])

Initial Latency for Variable Latency setting (CR [3]=0) is LC or 2LC , based on Refresh Collision like below table. So host chipset must monitor DQSM signal, which indicates Refresh Collision occurrence or not. But Initial Latency for Fixed Latency setting (CR [3] = 1) is always 2LC.

Table 6.5 Variable Latency (CR[3] = 0)

| Latency code CR[7:4] | Initial Latency Counter | | Maximum Operating Frequency (Mhz) | |
|-------------------------|-----------------------------------|-------------------------|--------------------------------------|------|
| | No Refresh Collision (LC) | Refresh Collision (2LC) | 1.8V | 3.0V |
| 0000 | 3 clocks | 6 clocks | 83 | |
| 0001 | 4 clocks | 8 clocks | 100 | |
| 0010 | 5 clocks (default at 3V) | 10 clocks | 133 | |
| 0011 | 6 clocks | 12 clocks | 133 | |
| 0100 | 7 clocks | 14 clocks | NA | |
| 0101 | 8 clocks (default at 1.8V) | 16 clocks | 166Mhz | 133 |
| 0100 - 1111 | Reserved | - | NA | |

Notes: Default setting for 1.8V device is “0101”, and that for 3.0V device is “0010”.

Table 6.6 Initial Latency Summary Table⁽¹⁾

| Destination | Operating mode | Variable mode (default) initial Latency Count | | Fixed mode Initial Latency Count |
|-------------|----------------|--|--------------------------|-------------------------------------|
| | | No Refresh Collision | Refresh Collision | |
| Memory | READ | 1LC | 2LC | 2LC |
| | WRITE | 1LC | 2LC⁽²⁾ | 2LC⁽²⁾ |
| Register | READ | 1LC | 2LC⁽²⁾ | 2LC⁽²⁾ |
| | WRITE | 0LC | | 0LC |

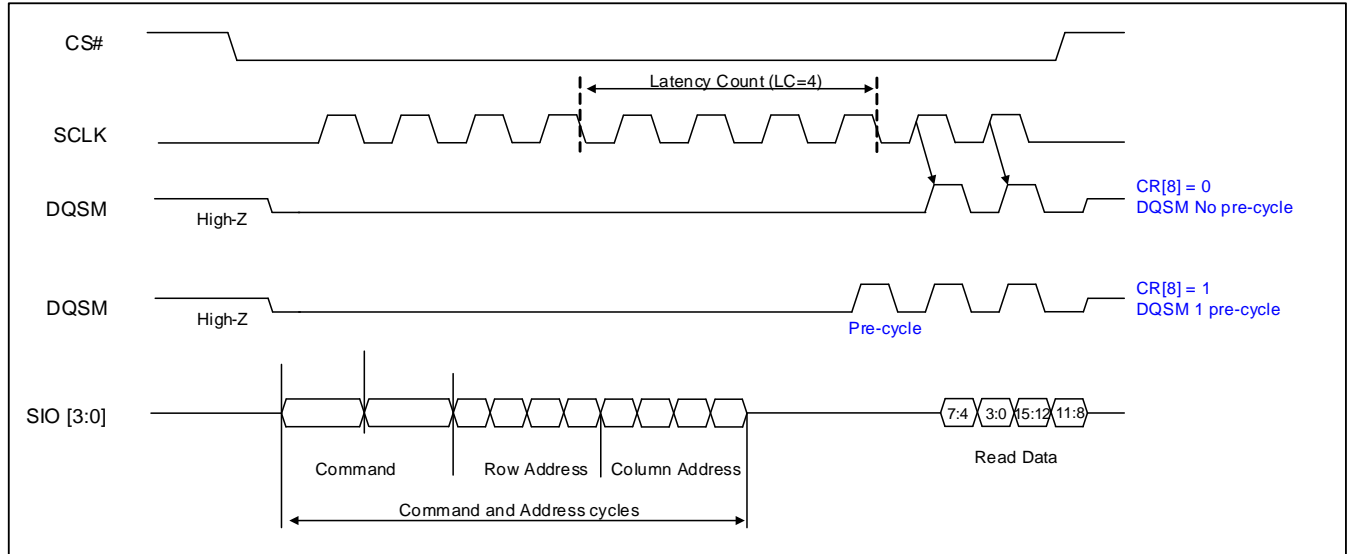
Notes:

1. LC means Latency Counter clocks, which is in Configuration Register Bit [7:4], as defined in ["Table 6.1"](#) and ["Table 6.3"](#).
2. Contact ISSI MKT if 1LC is required instead of 2LC.

6.2.3 DQSM READ Pre-Cycle (CR [8])

CR [8] defines DQSM Pre-Cycle.

Figure 6.3 DQSM pre-cycle Timing, No Refresh Collision at Variable Latency READ (1LC operation)



Notes:

1. Latency count (LC) is 4 clocks.
2. When Configuration Register bit [8] = 0, the Device will output DQSM with valid data cycle.
3. When Configuration Register bit [8] = 1, the Device will output 1 pre-cycle (dummy DQSM) prior to valid data cycle.
4. The memory drives DQSM during read cycles.

6.2.4 Deep Power Down (CR [15])

CR [15] defines DQSM Pre-Cycle.

Figure 6.4 Deep Power Down Entry Timing

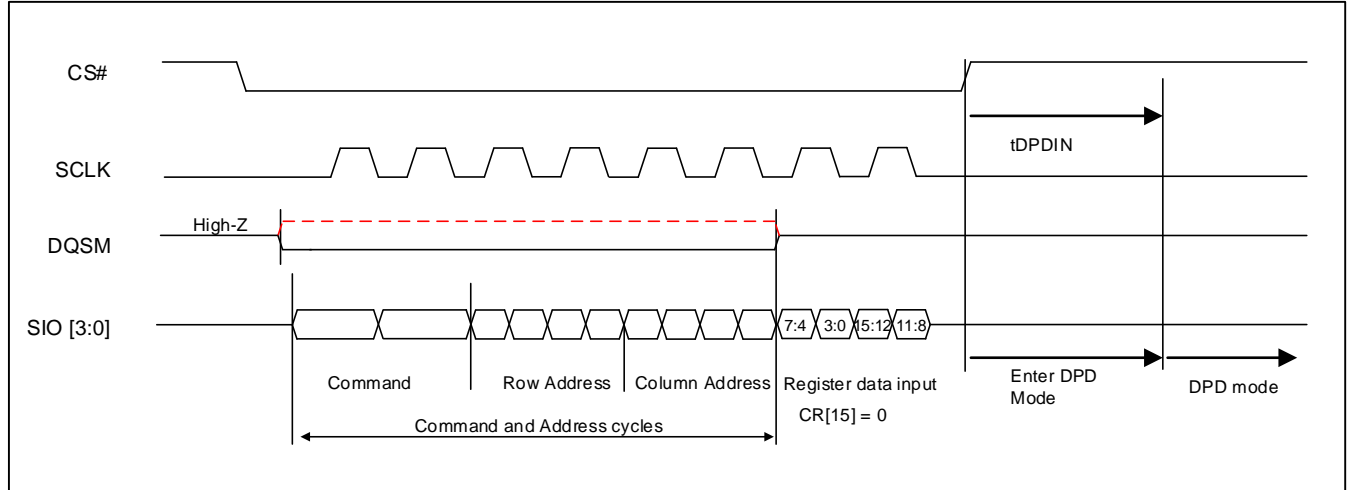
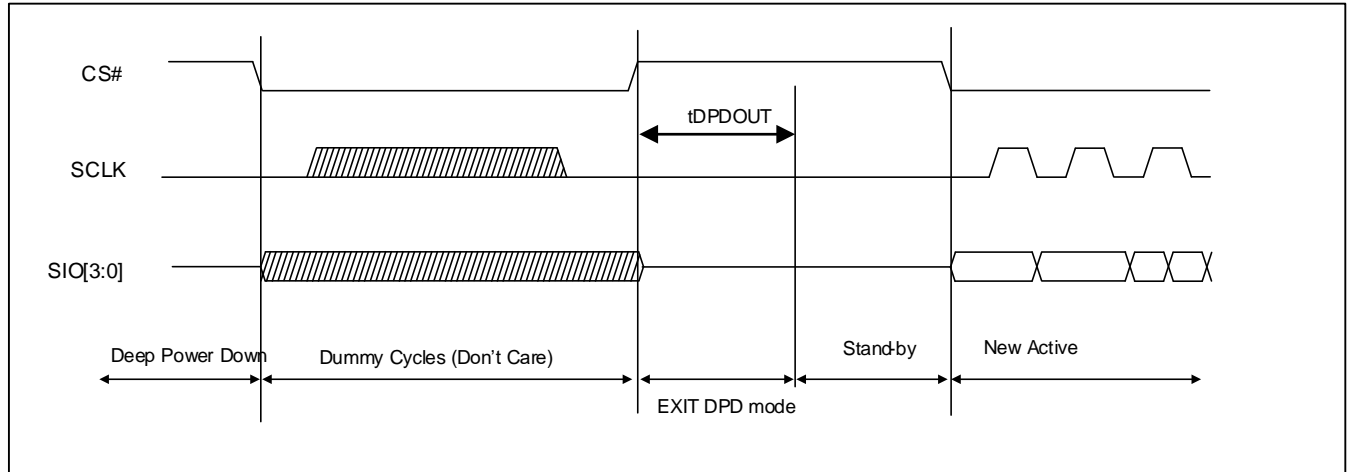


Figure 6.4 Deep Power Down Exit Timing



Note: Memory Cell Data cannot be retained at deep power down (DPD) mode.

Table 6.7 Deep Power Down Timing Parameters

| Parameter | Description | Min | Max | Unit |
|-----------|--|-----|-----|------|
| tDPDIN | Deep Power Down CR[15]=0 register write to DPD power level | 150 | - | us |
| tDPDX | CS# Low period to exit from Deep Power Down | 200 | - | ns |
| tDPDOUT | CS# Low then High to Standby wakeup time | - | 150 | us |

6.3 DEVICE IDENTIFICATION REGISTER

It is a read only, non-volatile, word register that provides device information. The device information fields can be identified as below.

- a. Device Type
- b. Density
 - i. Row address bit count
 - ii. Column address bit count
- c. Manufacturer

Table 6.8 ID Register

| Bits | Function | Settings (Binary) |
|---------|--------------------------|---|
| 15 - 13 | Device Voltage | 000: 1.8V 001: 3V |
| 12 - 8 | Row address bit count | 00000 : 1 row address 01100 : 13 row address 11111 : 32 row address |
| 7 - 4 | Column address bit count | 0000 : 1 column address 0110: 7 column address 1111 : 16 column address |
| 3 - 0 | Manufacturer | 0011 (ISSI) |

6.4 ECC REGISTER

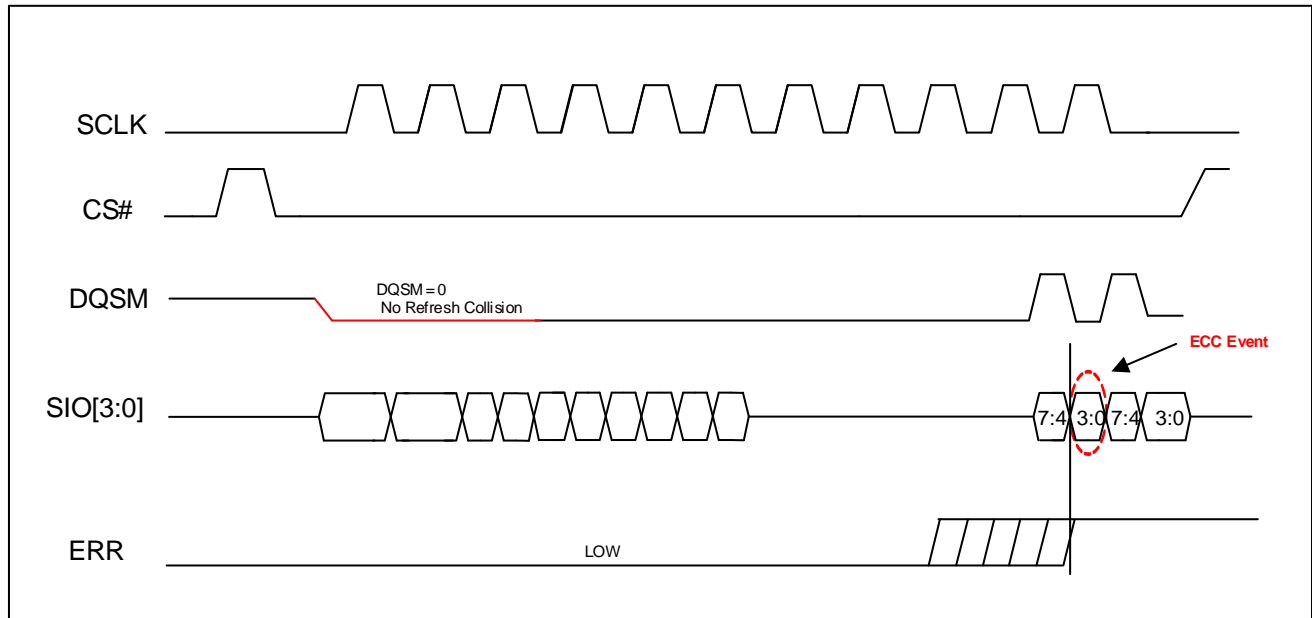
It is to set ECC related configuration. The ECC Register information fields can be identified as below.

- a. ECC ON/OFF
- b. ERR signal ON/OFF: ERR signal is active only when ECC is ON. It enables customer to monitor real time ECC Event occurrence. It is output only signal, so it can be left floating when it is not used. When ECC event occurred at specific read data, ERR signal goes high same time with spec read data or earlier than specific read data.
When ERR signal goes high, it will remain high until clear bit (bit 9) sets to 1 or power ON-OFF/ RESET operation.
- c. ERR Indicator Type: It selects ERR signal behavior type.

Table 6.9 ECC Register

| Bit | Function | Settings (Binary) | |
|-------|----------------------------------|---|--------|
| 15 | ECC ON/OFF | 0- ECC OFF 1- ECC ON. (default) | R/W |
| 14 | ERR Output ON/OFF | 0- ERR OFF 1- ERR ON. (default, ERR can be ON when ECC is ON) | R/W |
| 13-12 | ERR Indication Type | 00 – 1-bit Error Correction 01 – 2-bit Error Detection 10 – Any kind of ECC Event (default) 11 - Reserved | R/W |
| 11 | 1-bit Error Correction History | 0 – No 1-bit Error Correction Event 1 – Yes 1-bit Error Correction Event | R only |
| 10 | 2-bit Error Detection History | 0 – No 2-bit Error Detection Event 1 – Yes 2-bit Error Detection Event | R only |
| 9 | Clear ECC History and ERR signal | 0 - default 1 – Clear Automatically return to “0” after Clear operation | R/W |
| 8-0 | Reserved for Future Use | - | - |

Figure 6.5 ERR Timing when ECC Event occurred



Notes:

1. ERR signal goes Low after power-up when bit 14 (ERRON bit) and bit 15 (ECCON bit) in ECC register are ON regardless of CS#.
2. ECC chunk size is 4-bit, so ERR signal must go High no later than bit [3:0] out of ECC event occurred byte.
3. ERR signal is an asynchronous signal, and remains High after detecting ECC Event until being cleared by bit [9] of ECC register.
4. ERR signal is an optional output signal, so it can be left floating (or disabled by bit [14] of ECC Register)

6.5 IN BAND RESET

The device offers an additional feature of In-Band RESET function, which uses existing SPI signals to initiate a hardware reset, which is different from existing software reset/hardware reset (dedicated RESET# pin);

- Existing software reset commands often depend on the Flash being in a particular mode before they are effective. This makes software based reset sequences depend on slave device and mode.
- Dedicated RESET# pin requires additional pin over traditional 8-pins of SPI device. Also it requires 1 more signal for reset operation.

In Band-RESET operation requires 2-signal pins; CS# and SIO0.

- CS# is driven active low to select the SPI slave (note1)
- Clock (SCLK) remains stable in either a high or low state(note 2)
- SIO0 is driven low by the bus master, simultaneously with CS# going active low.....(note 3)
- CS# is driven inactive ... (note 4)
- Repeat the above 4 steps, each time alternating the state of SIO0.
- After the fourth CS# pulse, the slave triggers its internal reset.....(note 5)

Note 1 This powers up the SPI slave

Note 2 This prevents any confusion with a command, as no command bits are transferred (clocked)

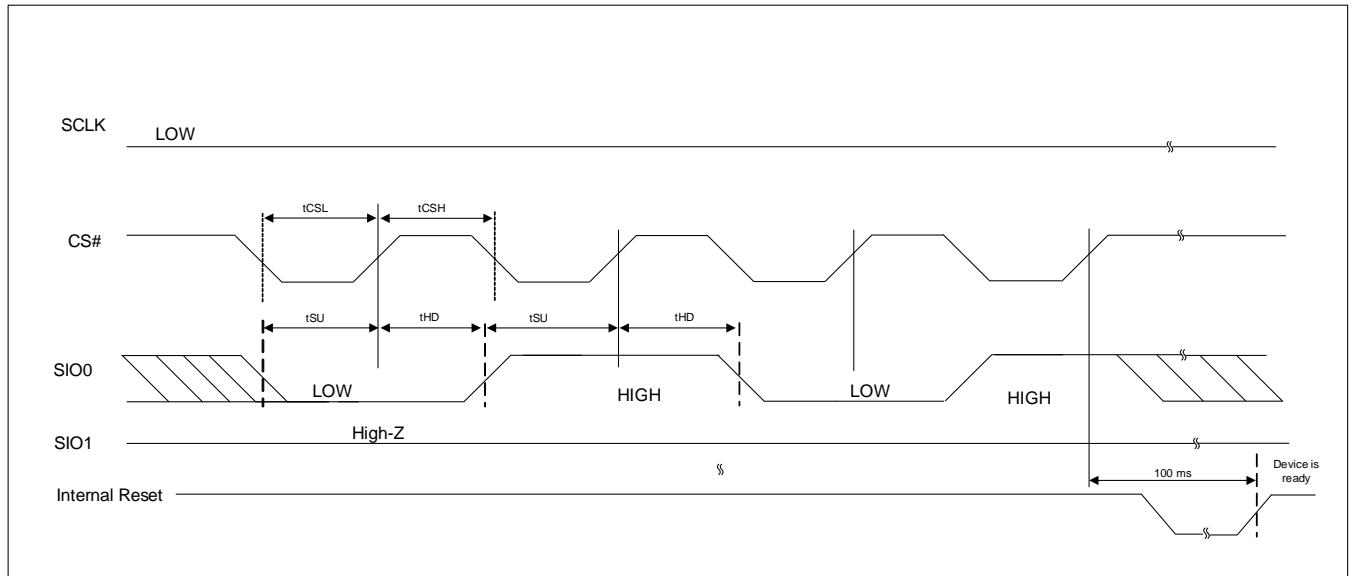
Note 3 No SPI bus slave drives SIO0 during CS# low before a transition of clock. Slave streaming output active is not allowed until after the first edge of clock.

Note 4 The slave captures the state of SIO0 on the rising edge of CS#

Note 5 SIO0 is low on the first CS#, high on the second, low on the third, high on the fourth ... (This provides a 5th, unlike random noise)

NOTE:

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. During the reset process, the device will ignore any chip select (command).

Figure 6.6 Timing for In-Band RESET Operation


| Parameter | Symbol | Min | Max | Units |
|----------------|-----------|-----|-----|-------|
| CS# Low Pulse | t_{CSL} | 500 | -- | ns |
| CS# High Pulse | t_{CSH} | 500 | -- | ns |
| Setup Time | t_{SU} | 5 | -- | ns |
| Hold Time | t_{HD} | 5 | -- | ns |

7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|---|------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Voltage with Respect to Ground on All Pins | -0.5V to $V_{CC} / V_{CCQ} + 0.5V$ |
| Voltage on V_{CC} supply relative to Ground | -0.5V to $V_{CC} + 0.5V$ |
| Voltage on V_{CCQ} supply relative to Ground | -0.5V to $V_{CCQ} + 0.5V$ |
| Electrostatic Discharge Voltage (Human Body Model) ⁽²⁾ | -2000V to +2000V |

Notes:

1. Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. ANSI/ESDA/JEDEC JS-001

7.2 OPERATING RANGE

| | | |
|-----------------------|---------------------|--|
| Operating Temperature | Industrial Grade | -40°C to 85°C |
| | Automotive Grade A2 | -40°C to 105°C |
| V_{CC} Power Supply | IS66/67WVQ4M4EDALL | 1.70V (V _{MIN}) –1.95V (V _{MAX}); 1.8V (Typ) |
| | IS66/67WVQ4M4EDBLL | 2.7V (V _{MIN}) –3.6V (V _{MAX}); 3.0V (Typ) |

7.3 DC CHARACTERISTICS

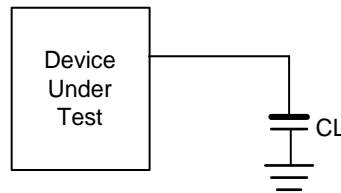
| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|----------------|--|----------------|------|----------------|-------|---|
| I_{LI} | Input Leakage Current 3V Device Reset Signal Only | - | - | ±10.0 | uA | VIN = VSS to VCC, VCC = VCC max |
| I_{LI} | Input Leakage Current 1.8V Device Reset Signal Only | - | - | ±5.0 | uA | VIN = VSS to VCC, VCC = VCC max |
| I_{CC1} | VCC Active Read Current | - | - | 18 | mA | CS# = VIL, @166MHz, VCC = 1.9V |
| | | | - | 15 | | CS# = VIL, @133MHz, VCC = 3.6V |
| I_{CC2} | VCC Active Write Current | - | - | 18 | mA | CS# = VIL, @166MHz, VCC = 1.9V |
| | | | - | 15 | | CS# = VIL, @133MHz, VCC = 3.6V |
| I_{CC4I} | VCC Standby Current at -40°C to +85°C | - | - | 200 | uA | CS#, VCC=VCC max |
| I_{CC4IP} | VCC Standby Current at -40°C to +105°C | - | - | 300 | | |
| I_{CC5} | Reset Current | - | - | 20 | mA | CS# = VIH, RESET# = VSS +/- 0.3V, VCC = VCC max |
| I_{CC6I} | Active Clock Stop Current at -40°C to +85°C | - | - | 8 | mA | CS# = VIL, RESET# = VCC +/- 0.3V, VCC = VCC max |
| I_{CC6IP} | Active Clock Stop Current at -40°C to +105°C | - | - | 12 | | |
| I_{CC7} | VCC Current during power up | - | - | 35 | mA | CS#, = H, VCC= VCC max, VCC=VCCQ= 1.95V or 3.6V |
| I_{DPD} | Deep Power Down Current 3V | - | - | 30 | uA | CS#, VCC = 3.6V, -40°C to +85°C |
| | Deep Power Down Current 1.8V | - | - | 20 | | CS#, VCC = 1.9V, -40°C to +85°C |
| I_{DPDP} | Deep Power Down Current 3V | - | - | 50 | uA | CS#, VCC = 3.6V, -40°C to +105°C |
| | Deep Power Down Current 1.8V | - | - | 30 | | CS#, VCC = 1.9V, -40°C to +105°C |
| $V_{IL}^{(1)}$ | Input Low Voltage | -0.5 | | $0.3V_{CC}$ | V | |
| $V_{IH}^{(1)}$ | Input High Voltage | $0.7V_{CC}$ | | $V_{CC} + 0.3$ | V | |
| V_{OL} | Output Low Voltage | | | 0.2 | V | $I_{OL} = 100 \mu A$ |
| V_{OH} | Output High Voltage | $V_{CC} - 0.2$ | | | V | $I_{OH} = -100 \mu A$ |

Notes:

- Maximum DC voltage on input or I/O pins is VCC + 0.5V. During voltage transitions, input or I/O pins may overshoot VCC by +2.0V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -2.0V for a period of time not to exceed 20ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc (Typ), TA=25°C.

7.4 AC MEASUREMENT CONDITIONS

| Symbol | Parameter | Min | Max | Units |
|--------|----------------------------------|------------------------|-----|-------|
| CL | Output Load Capacitance | | 20 | pF |
| TR,TF | Input Rise and Fall Times | 2 | | V/ns |
| VIN | Input Pulse Voltages | 0V to V _{CCQ} | | V |
| VREFI | Input Timing Reference Voltages | V _{CCQ} /2 | | V |
| VREFO | Output Timing Reference Voltages | V _{CCQ} /2 | | V |

Figure 7.1 Test Setup

7.5 PIN CAPACITANCE (TA = 25°C, VCC=1.8V/ 3V, 1MHZ)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---------------------|--------------------------------------|--------------------------|-----|-----|-----|-------|
| C _{IN} | Input Capacitance (CS#, SCLK) | V _{IN} = 0V | 3 | - | 4.5 | pF |
| C _{IN/OUT} | Input/Output Capacitance (SIO, DQSM) | V _{IN/OUT} = 0V | 3 | - | 4.0 | pF |

Note:

1. These parameters are characterized and not 100% tested.

7.6 AC CHARACTERISTICS
7.6.1 Read Timing Parameters (1.8V)

| Symbol | Parameter | 166MHz | | Unit | |
|--------|--|--------------|------|-------|----|
| | | Min. | Max. | | |
| LC | Latency Counter (No Refresh Collision) | 8 | - | clock | |
| tRWR | Read-Write Recovery Time | 48 | - | ns | |
| tCK | Clock(CLK) Period | 6 | - | ns | |
| tCH | Clock High level width | 0.45 | - | tCKmi | |
| tCL | Clock Low level width | 0.45 | - | tCKmi | |
| tHP | Clock half period | Min(tCH,tCL) | - | ns | |
| tDQSV | CS# Active to DQSM valid | - | 12 | ns | |
| tAC | Clock transition to DQ valid | 1 | 5.5 | ns | |
| tDQSCK | Clock transition to DQSM valid | 1 | 5.5 | ns | |
| tCSP | CS# High Between READ/WRITE | 6 | - | ns | |
| tCSS | CS# Setup to next CLK Rising Edge | 3 | - | ns | |
| tCSH | CS# Hold After CLK Falling Edge | 2 | - | ns | |
| tSS | SDR Input Setup | 1.0 | - | ns | |
| tSH | SDR Input Hold | 1.0 | - | ns | |
| tDS | DDR Input Setup | 0.6 | - | ns | |
| tDH | DDR Input Hold | 0.6 | - | ns | |
| tDQSQ | DQSM-DQ Skew | - | 0.45 | ns | |
| tQHS | Data Hold Skew factor | - | 0.85 | ns | |
| tQH | DQ hold time from DQSM | tHP-tQHS | - | ns | |
| tLZ | Clock to DQ Low-Z | 0 | - | ns | |
| tHZ | CS# Inactive to DQSM and DQ High-Z | - | 6 | ns | |
| tCSM | Chip Select Maximum Low Time | ~ 85°C | - | 4.0 | us |
| | | ~ 105°C | - | 1.0 | us |

7.6.2 Read Timing Parameters (3.0V)

| Symbol | Parameter | 133Mhz | | 100Mhz | | Unit | |
|--------|--|--------------|------|--------------|------|-------|----|
| | | Min. | Max. | Min. | Max. | | |
| LC | Latency Counter (No Refresh Collision) | 5 | - | 4 | - | clock | |
| tRWR | Read-Write Recovery Time | 37.5 | - | 40 | - | ns | |
| tCK | Clock(CLK) Period | 7.5 | - | 10 | - | ns | |
| tCH | Clock High level width | 0.45 | - | 0.45 | - | tCKmi | |
| tCL | Clock Low level width | 0.45 | - | 0.45 | - | tCKmi | |
| tHP | Clock half period | Min(tCH,tCL) | - | Min(tCH,tCL) | - | ns | |
| tDQSV | CS# Active to DQSM valid | - | 12 | - | 12 | ns | |
| tAC | Clock transition to DQ valid | 2 | 7 | 2 | 7 | ns | |
| tDQSCK | Clock transition to DQSM valid | 2 | 7 | 2 | 7 | ns | |
| tCSP | CS# High Between READ/WRITE | 7.5 | - | 10 | - | ns | |
| tCSS | CS# Setup to next CLK Rising Edge | 3 | - | 3 | - | ns | |
| tCSH | CS# Hold After CLK Falling Edge | 2 | - | 2 | - | ns | |
| tSS | SDR Input Setup | 1.2 | - | 1.5 | - | ns | |
| tSH | SDR Input Hold | 1.2 | - | 1.5 | - | ns | |
| tDS | DDR Input Setup | 0.8 | - | 1.0 | - | ns | |
| tDH | DDR Input Hold | 0.8 | - | 1.0 | - | ns | |
| tDQSQ | DQSM-DQ Skew | - | 0.75 | - | 0.8 | ns | |
| tQHS | Data Hold Skew factor | - | 0.90 | - | 0.95 | ns | |
| tQH | DQ hold time from DQSM | tHP-tQHS | - | tHP-tQHS | - | ns | |
| tLZ | Clock to DQ Low-Z | 0 | - | 0 | - | ns | |
| tHZ | CS# Inactive to DQSM and DQ High-Z | - | 7 | - | 7 | ns | |
| tCSM | Chip Select Maximum Low Time | ~ 85°C | - | 4.0 | - | 4.0 | us |
| | | ~ 105°C | - | 1.0 | - | 1.0 | us |

7.6.3 WRITE Timing Parameters (1.8V)

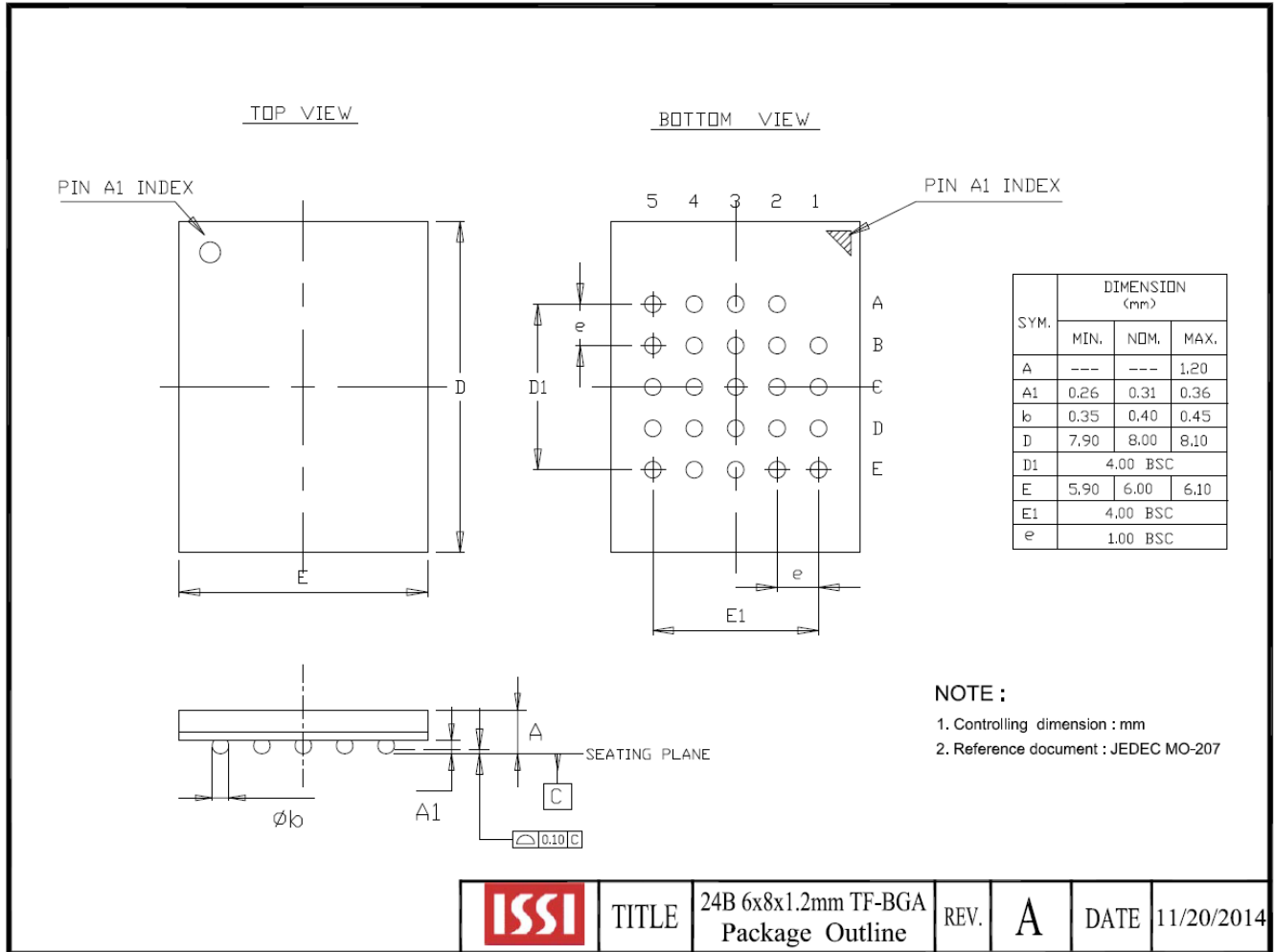
| Symbol | Parameter | 166MHz | | Unit | |
|--------|---|--------------|------|--------|----|
| | | Min. | Max. | | |
| LC | Latency Counter (No Refresh Collision) | 8 | - | clock | |
| tRWR | Read-Write Recovery Time | 48 | - | ns | |
| tCK | Clock(CLK) Period | 6 | - | ns | |
| tCH | Clock High level width | 0.45 | - | tCKmin | |
| tCL | Clock Low level width | 0.45 | - | tCKmin | |
| tHP | Clock half period | Min(tCH,tCL) | - | ns | |
| tDQSV | CS# Active to DQSM valid | - | 12 | ns | |
| tDQSCK | Clock transition to DQSM valid | 1 | 5.5 | ns | |
| tCSP | CS# High Between READ/WRITE | 6 | - | ns | |
| tCSS | CS# Setup to next CLK Rising Edge | 3 | - | ns | |
| tCSH | CS# Hold After CLK Falling Edge | 2 | - | ns | |
| tSS | SDR Input Setup | 1.0 | - | ns | |
| tSH | SDR Input Hold | 1.0 | - | ns | |
| tDS | DDR Input Setup | 0.6 | - | ns | |
| tDH | DDR Input Hold | 0.6 | - | ns | |
| tDMV | Data Mask Valid (DQSM setup to end of initial latency) | 0 | - | ns | |
| tCSM | Chip Select Maximum Low Time | ~ 85°C | - | 4.0 | us |
| | | ~ 105°C | - | 1.0 | us |

7.6.4 WRITE Timing Parameters (3.0V)

| Symbol | Parameter | 133Mhz | | 100Mhz | | Unit | |
|--------|---|--------------|------|--------------|------|--------|----|
| | | Min. | Max. | Min. | Max. | | |
| LC | Latency Counter (No Refresh Collision) | 5 | - | 4 | - | clock | |
| tRWR | Read-Write Recovery Time | 37.5 | - | 40 | - | ns | |
| tCK | Clock(CLK) Period | 7.5 | - | 10 | - | ns | |
| tCH | Clock High level width | 0.45 | - | 0.45 | - | tCKmin | |
| tCL | Clock Low level width | 0.45 | - | 0.45 | - | tCKmin | |
| tHP | Clock half period | Min(tCH,tCL) | - | Min(tCH,tCL) | - | ns | |
| tDQSV | CS# Active to DQSM valid | - | 12 | - | 12 | ns | |
| tCSP | CS# High Between READ/WRITE | 7.5 | - | 10 | - | ns | |
| tCSS | CS# Setup to next CLK Rising Edge | 3 | - | 3 | - | ns | |
| tCSH | CS# Hold After CLK Falling Edge | 2 | - | 2 | - | ns | |
| tSS | SDR Input Setup | 1.2 | - | 1.5 | - | ns | |
| tSH | SDR Input Hold | 1.2 | - | 1.5 | - | ns | |
| tDS | DDR Input Setup | 0.8 | - | 1.0 | - | ns | |
| tDH | DDR Input Hold | 0.8 | - | 1.0 | - | ns | |
| tDMV | Data Mask Valid (DQSM setup to end of initial latency) | 0 | - | 0 | - | ns | |
| tCSM | Chip Select Maximum Low Time | ~ 85°C | - | 4.0 | - | 4.0 | uS |
| | | ~ 105°C | - | 1.0 | - | 1.0 | us |

8. PACKAGE TYPE INFORMATION

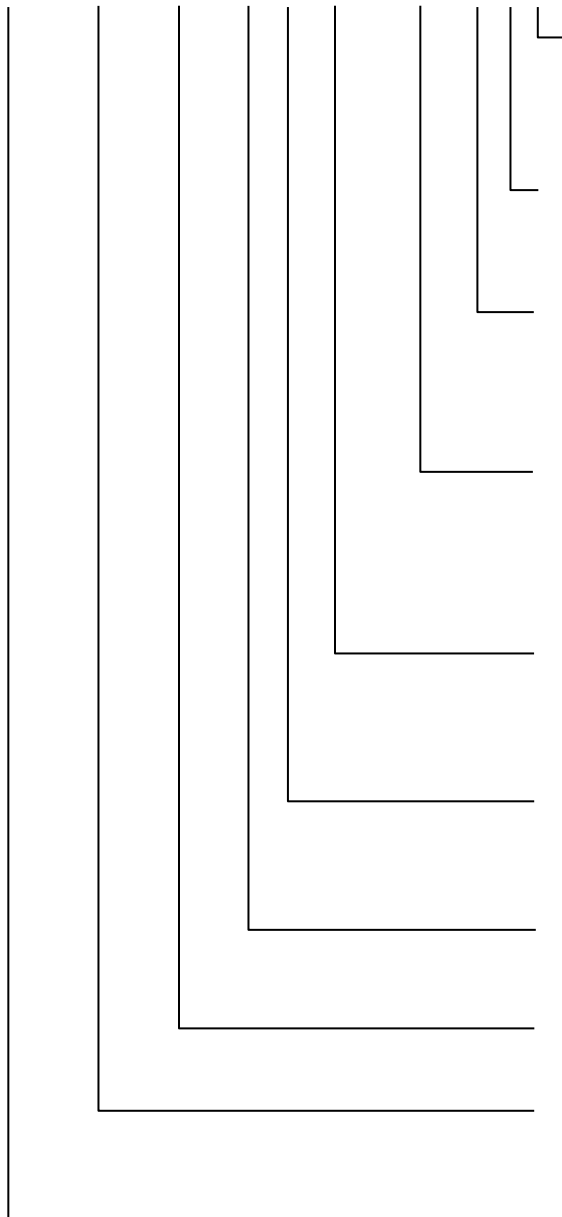
8.1 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 BALL ARRAY (B)



| | | | | | | |
|--|-------|--------------------------------------|------|---|------|------------|
| | TITLE | 24B 6x8x1.2mm TF-BGA Package Outline | REV. | A | DATE | 11/20/2014 |
|--|-------|--------------------------------------|------|---|------|------------|

9. ORDERING INFORMATION – Valid Part Numbers

IS66 WVQ 2M4 E D ALL - 166 B L I



TEMPERATURE RANGE

I = Extended (-40°C to +85°C)
 A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT

L = RoHS compliant

PACKAGE Type ⁽¹⁾

B = 24-ball TFBGA 6x8mm 5x5 ball array
 W = KGD (Call Factory)

Frequency

166 = 166MHz
 133 = 133MHz
 100 = 100MHz

VDD

ALL = 1.8V
 BLL = 3.0V

Die Revision

D = die rev D

On Chip ECC

E = On Chip ECC

Density/Org.

2M4 = 2Mb x 4 = 8Mb

PSRAM Product Type.

WVQ = QuadRAM

BASE PART NUMBER

IS = Integrated Silicon Solution Inc.

66 = PSRAM
 67 = PSRAM for Automotive

Industrial Temperature Range (-40°C to +85°C)

| Config. | Voltage | Package | Frequency (MHz) | Order Part Number |
|---------|---------|------------------------------------|-----------------|------------------------|
| 2Mbx4 | 1.8V | 24-ball TFBGA 6x8mm 5x5 ball array | 166 | IS66WVQ2M4EDALL-166BLI |
| | 3.0V | 24-ball TFBGA 6x8mm 5x5 ball array | 133 | IS66WVQ2M4EDBLL-133BLI |
| | | | 100 | IS66WVQ2M4EDBLL-100BLI |

Automotive A2 Temperature Range (-40°C to +105°C)

| Config. | Voltage | Package | Frequency (MHz) | Order Part Number |
|---------|---------|------------------------------------|-----------------|-------------------------|
| 2Mbx4 | 1.8V | 24-ball TFBGA 6x8mm 5x5 ball array | 166 | IS67WVQ2M4EDALL-166BLA2 |
| | 3.0V | 24-ball TFBGA 6x8mm 5x5 ball array | 133 | IS67WVQ2M4EDBLL-133BLA2 |
| | | | 100 | IS67WVQ2M4EDBLL-100BLA2 |