AN42S01.AN

ISSI SRAM/SDRAM Layout Guide

Application Note (AN42S01.AN)

Introduction

This is a general PCB layout guideline for ISSI SRAM/SDRAM, especially targeting for point to point application. Chipset companies may require for a special or additional guideline. ISSI recommends following the chipset company's rule first.

1. PCB Layout Guidelines

50–60Ω impedance e (ZO) is recommended for all traces. FR-4 is commonly used for the dielectric material. And its thickness and trace width and thickness should be adjusted for matching the impedance. Trace lengths are also important that should be determined through simulation for each signal group.

1. Signals from the same net group should be generally routed on the same layer. Net groups are divided into clock (if it is a sync product), Address, DQ and DM(if DQ is separated, D and Q are considered as different group), and Command and controls.
2. Minimum rules are generally accepted as below.
   -. Minimum trace width is 0.13mm(5mil).
   -. Intranet spacing, the distance between two adjacent traces within a net, is 0.2mm(7mil).
   -. Internet spacing, the distance between the two outermost signals of different signal group is 0.381mm(15mil).
3. Keep all data bus in same layer of the board, and place them on different layers from address and control lanes, if possible. If data/ address/control lines are on the same layer, they must be isolated from each other by at least 0.381mm(15mil) to reduce crosstalk.
4. Maximum trace length is 2inches.
5. The longest-to-shortest trace length difference in each group must be ≤ 20.32mm(800mil) and this is from pin to pin.

2. Termination

Series termination will reduce overshoot and undershoot without additional power. Finding the best size of resistor is difficult and should be done by simulation. ISSI recommends 10~33Ω serial resistor termination on signals as a good example for the beginning of design. Resistor location should be closed to the transmitting device. If it is bidirectional pins like DQ, resistance should be located in the half way. As long as signals are in a good shape, termination is not required.

3. LAND Pattern

ISSI suggests adhering to IPC-7351 guidelines. For BGA components, the land diameter should not exceed the contact or ball diameter on the package, usually around 80% of the nominal ball size of the BGA. For alternative packages utilizing leads, such as TSOP or SOIC, the width of the land pattern is equal to or greater than the lead width.

For any question, please contact the ISSI Application Team.