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ISSI DDR4 SDRAM Layout Guide

Application Note (AN43QR001)

Introduction

This is a general PCB layout guideline for ISSI DDR4 SDRAM, especially for point-to-point applications. Chipset companies may have additional guidelines or requirements to use DDR4 with their DRAM controller. In such cases, ISSI recommends that those guidelines serve as primary, while these guidelines be considered as supplementary.

It is strongly encouraged that the board designer(s) consider all aspects of the board, such as signal integrity, electrical timings, etc., by using simulation models prior to board fabrication. After the board has been produced and completed with components, it is also recommended to further verify signal integrity and full functionality of the application.

PCB Layout Guidelines

FR-4, is commonly used as a dielectric material. The thickness and trace widths should be adjusted for optimal impedance. Propagation delays and trace lengths are also important and should be confirmed with simulations for each signal group. In general, ISSI recommends minimum design rules for PCB layout as defined below, for peak performance and to minimize signal distortion/crosstalk.

1. Decoupling Guidelines:

Guideline Notes:			
VDD		Minimum of two decoupling capacitors to VSS per SDRAM	Should be placed as close as possible to the DRAM VDD ball
		Minimum of one decoupling capacitor to VDD per every two termination resistors or a decoupling capacitor at both ends of each resistor network	
VTT			Should be placed as close as possible to the termination resistors
VPP		Minimum of one decoupling capacitor to VSS per DRAM ball	Should be placed as close as possible to the DRAM VPP ball
VREFCA		Minimum of one decoupling capacitor to VDD per DRAM	Should be placed as close as possible to the DRAM VREFCA ball
Note 1 Decoupling capacitor values vary by module and may be staggered to achieve best overall impedance vs. frequency response.			
Note 2 Recommended values for decoupling are 0.01 μ F, 0.1 μ F, and 1.0 μ F.			
Note 3 Recommended value for bulk decoupling is 4.7 μ F.			

1.1 Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. For high speed bypassing, select the required capacitance with the smallest package.

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2. Signal Groups:

Signal Groups are:

2.1 Clock (CK)

2.2 Address, Bank Address, Bank Group, Command and Control (ADD/CMD/CTRL)

2.4 Data Bus (including ECC byte) (DQ)

3. Impedance Assignments by Signal Type:

3.1 Signals from the same Byte group, such as DQS, DM and bits of DQ, should be routed in the same layer, if possible. If a layer transition is necessary, return current paths should be minimized to reduce inductance and impedance discontinuities. Optimizing Stitching VIAs and Bypass Capacitors will also help to minimize impedance discontinuities, which reduces crosstalk and signal distortion.

3.2 The DQ/DMI/DQS signals must be routed in inner layers with the same number of VIAs and barrel lengths to minimize trace crosstalk. DQ and DMI traces are recommended to be controlled to $\sim 40\Omega$

3.3 Propagation (Trace) delay must be carefully evaluated and controlled for the respective groups. Package delays should also be included in simulations to insure timing budgets have adequate margin in the application.

3.4 Trace impedance recommendations & thickness:

Signal Type	Impedance	Trace Width	
		Minimum	Nominal
CLOCK	70 Ω differential	0.1mm	0.15mm - 0.25mm
ADD/CMD/CTRL	40 Ω	0.1mm	0.15mm
DQ	50 Ω	0.1mm	0.15mm
DQS	83 Ω differential	0.1mm	0.15mm

Impedances for DDR4:

3.4.1 50 $\Omega \pm 10\%$ (typically achieved with 0.10 mm trace widths)

3.4.2 40 $\Omega \pm 10\%$ (typically achieved with 0.15 mm trace widths)

Differential impedances for DDR4:

3.4.3 83 $\Omega \pm 15\%$ (typically achieved with 0.10 mm trace widths with a 0.10 mm space)

3.4.4 70 $\Omega \pm 15\%$ (typically achieved with 0.15 mm trace widths with a 0.10 mm space)

3.5 The chipset manufacturer requires that each DDR4 package be located within a certain distance. Please contact with chipset vendor for further details.

4. Routing Space Constraints:

Feature	Preferred (mm)	Comment
Pad to pad spacing for pads of different components that are soldered down	0.250	Concern is solder bridging
Line to pad spacing	0.125	
Line to line spacing (single ended)	0.100	
Line to line spacing (differential)	0.100	
Line to shape spacing	0.200	
Shape to shape spacing	0.200	
Via to BGA pad	0.175	Copper to copper
Via to non-BGA pad	0.150	Copper to copper
Via to Via	0.200	Copper to copper
Minimum trace width on outer layers	0.090	
Minimum trace width on inner layers	0.075	

- 4.1 Clocks should be routed on the top layer for optimal signal quality without VIA's. They should maintain >5W spacing from other signals.
- 4.2 Differential clocks should be routed in parallel, with trace lengths as short as possible.
- 4.3 Terminations for differential clocks will use two resistors, one connected to each side: the true signal and the complementary signal for the differential pair. The other side of each resistor should be connected together and to a capacitor. The other side of the capacitor will be connected to the reference plane for the differential pair. This will be VDD and the capacitor value should be 0.01 μ F.
- 4.4 DDR4 offers programmable drive strength to match the impedance of I/O BUS. Seven drive strengths are supported: RZQ/7, RZQ/6, RZQ/5, RZQ/4, RZQ/3, RZQ/2 and RZQ/1.
This feature can avoid using any termination of I/O BUS to help improve power consumption and conserve space.
- 4.4 The DDR4 RZQ feature minimizes process variations that may be present in the driver. To calibrate output driver impedance, RZQ needs to be located between the ZQ ball and VDDQ. The value of RZQ must be $240\Omega \pm 1\%$.
- 4.5 ISSI recommends that the RESET pin on DDR4 is tied to VSS through an appropriate value resistor for the number of loads to maintain $0.2 \times VDD$ during power up.
- 4.6 ISSI recommends that the ODT pin on DDR4 be tied to VTT through a $33\Omega - 39\Omega$ resistor.
- 4.7 ISSI recommends if CA Parity feature is used, terminate PAR pin to VTT through a $33\Omega - 39\Omega$ resistor.
- 4.8 ISSI recommends that ALERT# pin on DDR4 be tied to VTT through a $33\Omega - 39\Omega$ resistor.
- 4.9 ISSI recommends that the TEN pin on DDR4 be tied to GND through a $1K \Omega$ resistor.

LAND pattern

Follow IPC-SM-782 and IPC-7351, and target the size of land pattern to be equal to 80% of the ball size of BGA.

For any question, please contact the ISSI Application Team.