

Quality Assurance

1. Quality Assurance in the Project Approval Stage

Before starting product planning, it is essential to carry out market research activities to ascertain the intended applications and the product quality/reliability demanded by each customer, and also to understand technical trends in the general marketplace, basic specifications, delivery requirements, prices, quality, reliability and other demands on products.

Information on demanded quality and reliability acquired through the above activities, various data obtained in-house from accumulated results and fundamental research on reliability technology are used to set target levels which are appropriate for product applications and operating environments and to formulate development plans.

This information is then compiled into product plans, and design specifications are drawn up based on these product plans and summarized as input for design.

1.1 Quality Assurance in the Design and Development Stage

1.1.1 Product Development and Design

Product design is an extremely important process for ensuring high quality and reliability in semiconductor devices, and it is necessary to implement both built-in quality and built-in reliability.

Product design proceeds according to the design specification. These specifications include design inputs (applicable regulations, customer demands and in-house standards) to ensure that appropriate requirements are considered. Product design goes through the stages of logic/circuit design, layout, mask design, prototype manufacture and evaluation before reaching completion.

1.1.2 Design Review

Design review consists of checking whether the design standards are the rules to be followed. Observance of design standards is checked using various simulation tools automatically or manually.

ISSI provides simulation models for each SRAM, DRAM, Flash and Analog part manufactured. These models are revised as new device and technologies are developed. Models can be obtained by contacting ISSI FAE department.

In addition, characterization data on each device are performed and retained in

ISSI K2 database. These characterization data are available upon request on a case-by-case basis.

1.1.3 Product Release

The final stage before a new product is released to manufacturing is Product Release. During the final product release meeting all requirements of the NPCL are reviewed for completeness and the checklist of items for the product released are discussed. When all are supplied of the satisfaction of the team, the documentation is signed off and the product is officially released together with the qualification and characterization data to demonstrate that the product can be manufactured in accordance to requirements.

1.1.4 Production Part Approval Process (PPAP)

As part of the NPCL process, the requirements of the PPAP for automotive products are supplied whenever a product is being qualified for automotive applications.

ISSI will supply the Certificate of Design, Construction and Qualification (CoDC) as well as the Part submission Warrant (PSW) together with the various specific requirements by the automotive customer.

ISSI subcontractors (Fab and Assembly) also submit their own PPAP to ISSI for new technologies and processes.

2 Quality Assurance in the Production Stage

2.1 Wafer Processing

1) Wafer Process Technology

Since ISSI is one of the IC design leaders in the world, we serve hundreds of customers with different needs and applications. In order to satisfy all customers' needs, we offer the Memory, Logic and Analog products with leading-edge IC process technologies in 25nm, 30nm, 38nm, 40nm, 45nm, 55nm, 63nm, 72nm, 99nm, 0.11-micron, 0.13-micron, 0.15-micron and 0.18-micron generations as well as 0.35-micron, 0.5-micron for Analog products.

The process technology is developed in accordance with standardized methodologies. Each new technology must pass a rigorous qualification procedure based on typical industry standards before it is released to mass production.

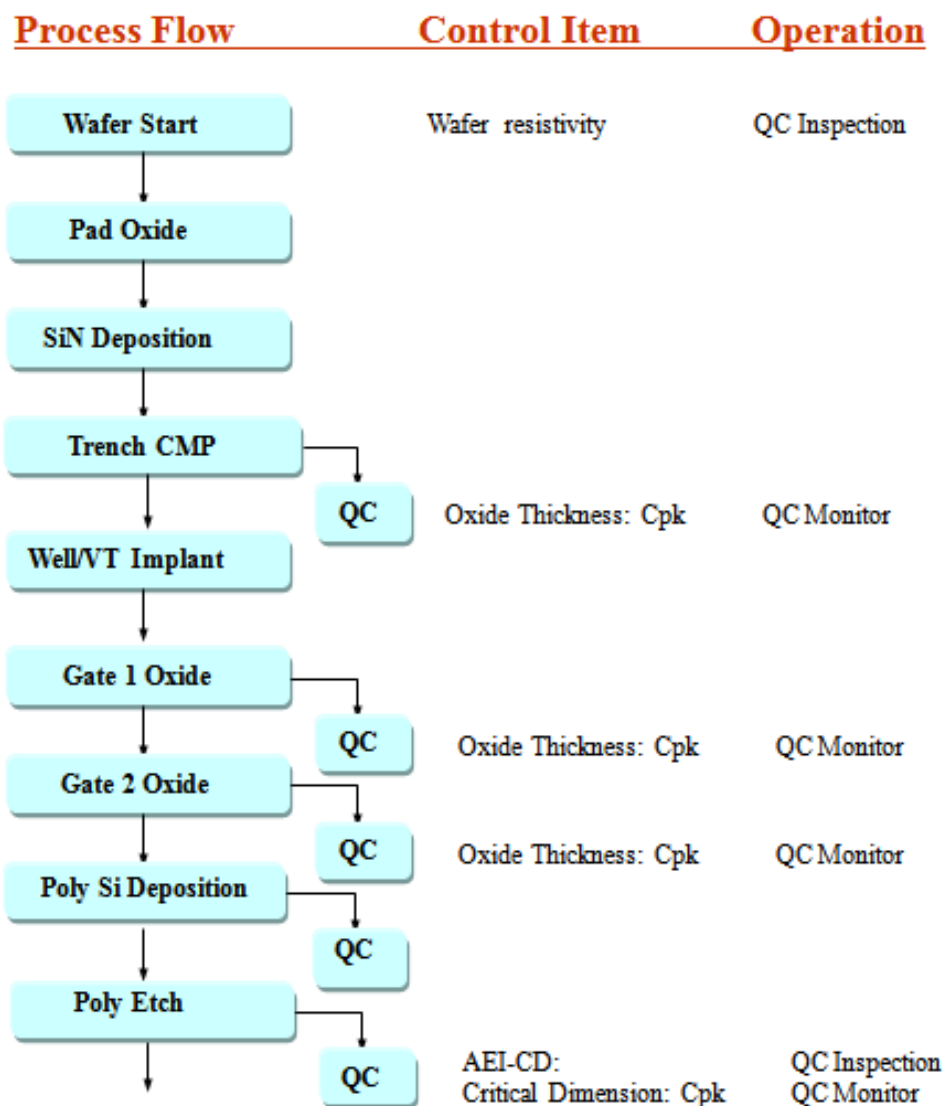
Once in production, every released process is constantly monitored against a predetermined set of standards. The monitor results are then published in the

foundry's website and ISSI QA will periodically access the database for evaluation.

Products released to production are monitored at the wafer and package level. Wafer acceptance test (WAT) data by lot indicate key process measurements tested to specified limits. Packaged units are periodically monitored for reliability based on package family and assembly line.

2) Wafer Process Flow and In-line Control

The generic wafer process flow and major control items are shown in Figure 3-1 with SRAM as an example.



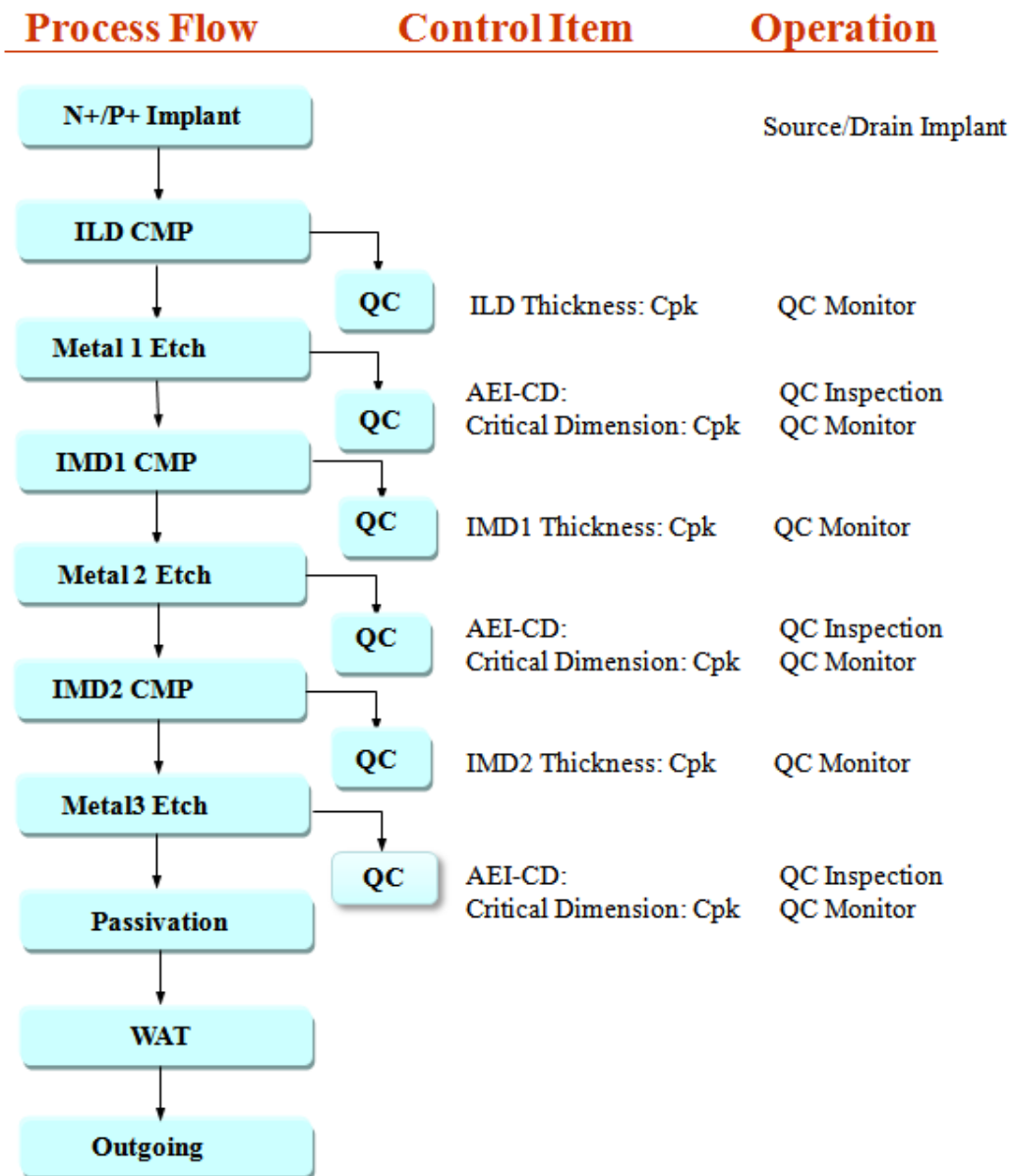
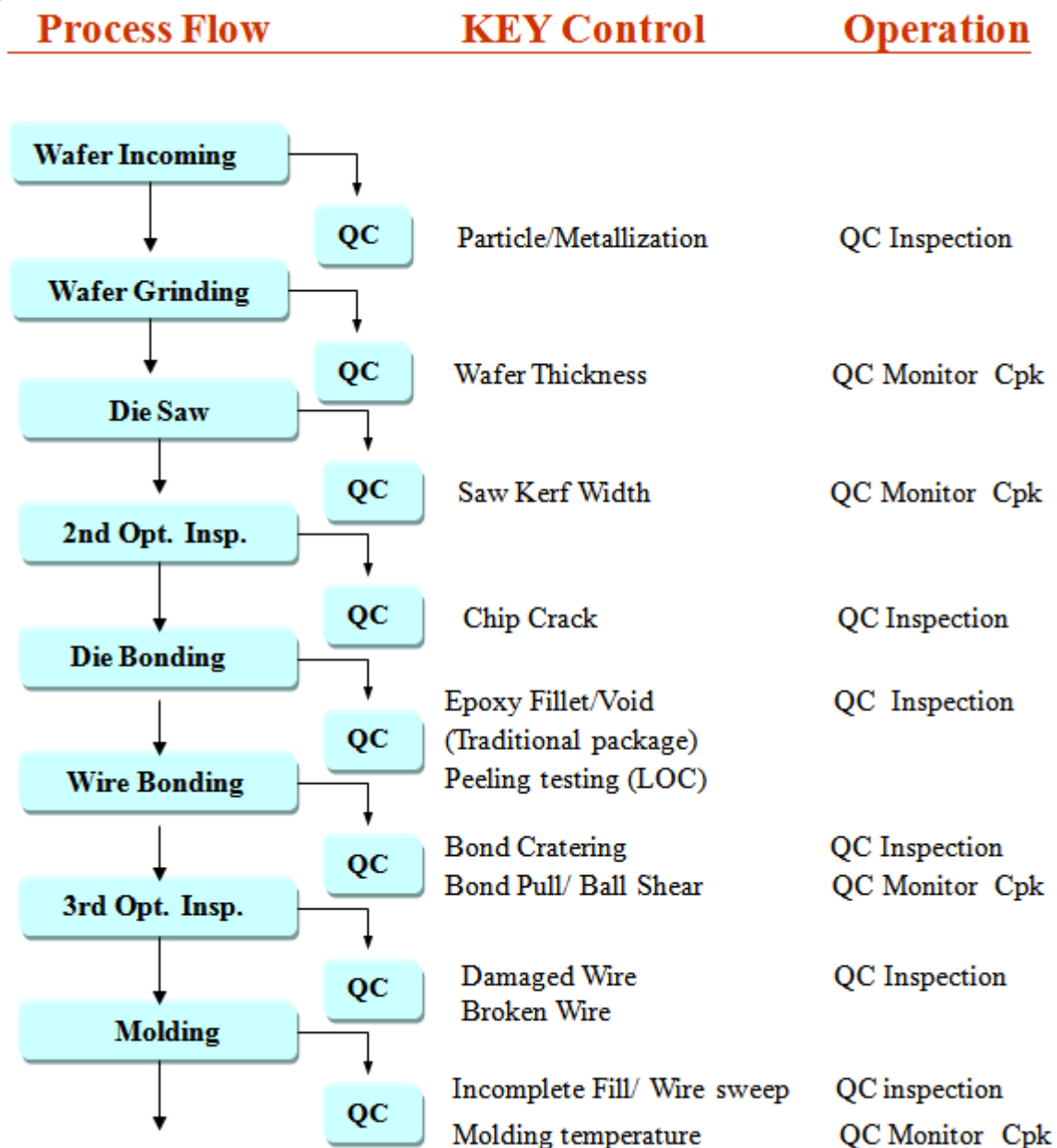


Figure 3.1 Generic SRAM Wafer Process & Control

2.2 Assembly Process Technology

Our qualified assembly houses offer IC packaging design and fabricate a full array of packages for ISSI products, with pin counts from 8 to more than 365. Major packaging offers include ball grid array (PBGA, TFBGA), quad flat packages (PQFP, TQFP, LQFP), small outline packages (SOP, TSOP, SOJ), PLCC and Dual/Quad flat no-lead (DFN.QFN) for Analog products. To ensure that they create world-class packages, the major assembly houses are ISO 9000, TS16949 and ISO 14001 certified companies.

The generic assembly process flow and major control item are shown in Figure 3-2.



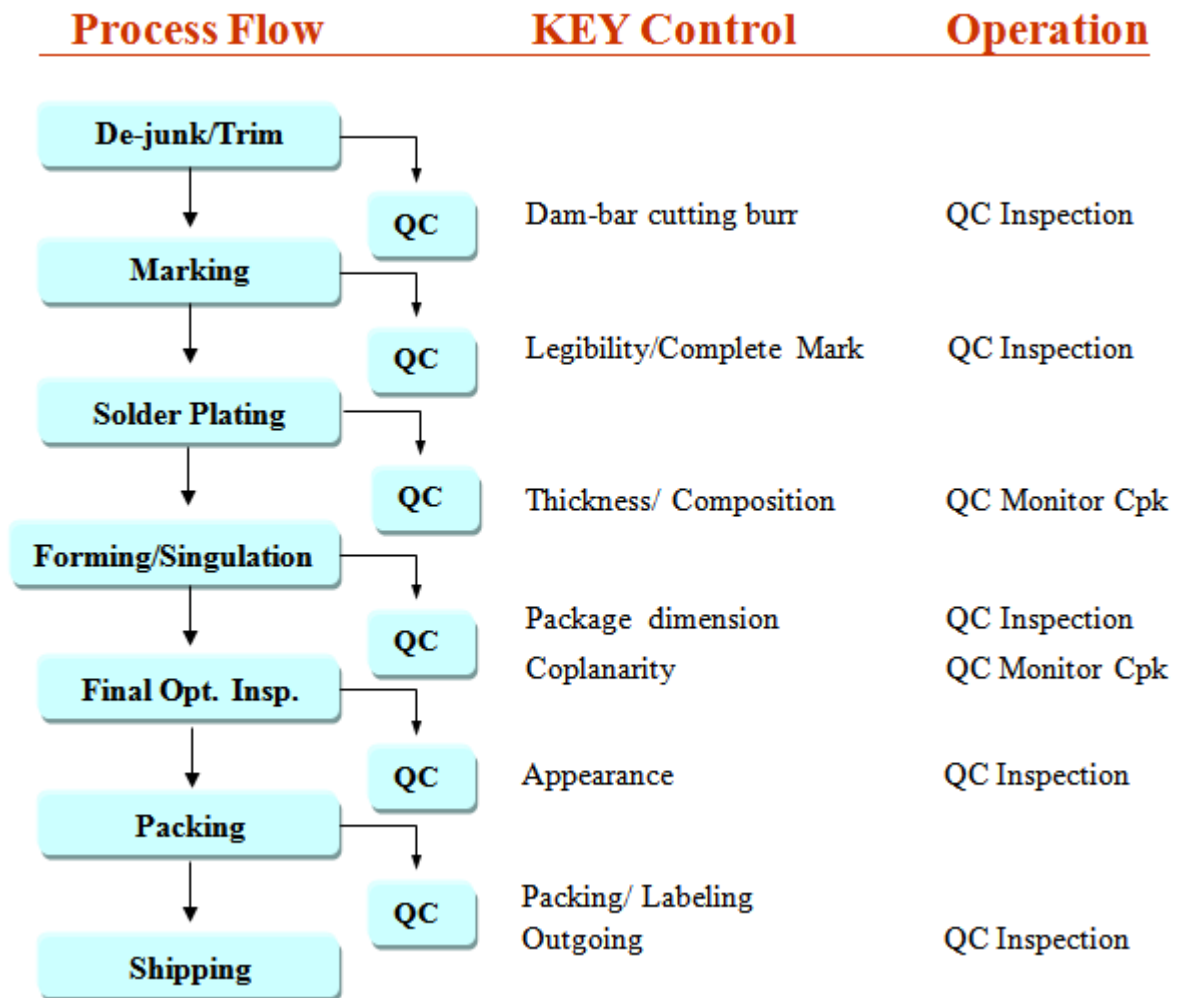


Figure 3-2 Generic Assembly Process & Control

2.3 Testing

1) Overview

The purpose of testing is to verify the conformance to ISSI specifications and/or customer requirements before the products are delivered to customers. Testing is an inspection process that is needed because the failures have not been eliminated. The failures are usually caused by design errors, materials and process defects, operational environment extremes, and aging effects.

Although testing does not add value to the product, ISSI recognizes it is crucial to recruit skilled engineering expertise to guarantee testing quality. This requires a sizable investment, however, we believe it is a necessity for any company intending to become, or remain as, a leading logic and memory supplier.

Electrical testing consists of three steps: 1) continuity test, 2) DC parametric test, and 3) functional and dynamic test (AC). It is used for verifying IC performance and conformance to ISSI published data sheet so that “bad” parts¹ are not shipped to the customers. The electrical specification limits and conditions are related to the wafer fabrication process parameters and thus to the potential physical defects that might occur.

2) SRAM/DRAM/Flash/Analog Product Testing Flow

The templates of Commercial SRAM, DRAM, Flash, Analog TEST Flow & Control are shown in Figures 3-3, 3-4 3-5 and 3-6 respectively.

3) Known Good Die Testing Flow

In addition to the package products ISSI offers die only material to customers. Known good Die (KGD) business and service is provided to our customers upon request. The generic KGD Test Flow and Control is shown in Figure 1-12.

These die could be in wafer form. Also, the customer can choose an option of tested die without speed testing (Known Tested Die) or die that had gone through burn-in and full testing (Known Good Die)

¹ The unit of measurement for this is typically a parts-per-million (ppm) value for the defective parts shipped to customer.

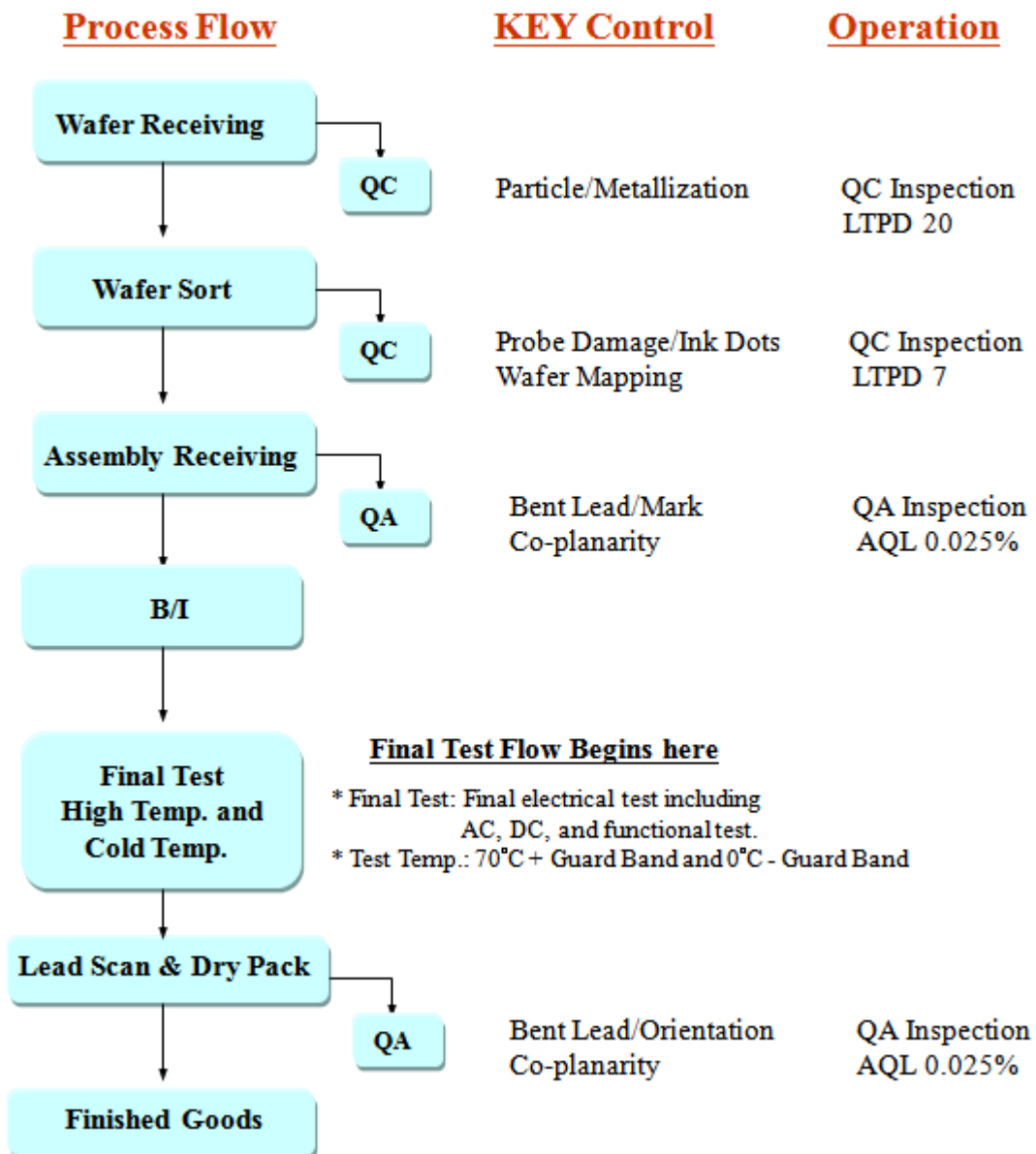


Figure 3-3 Commercial SRAM Test Flow & Control

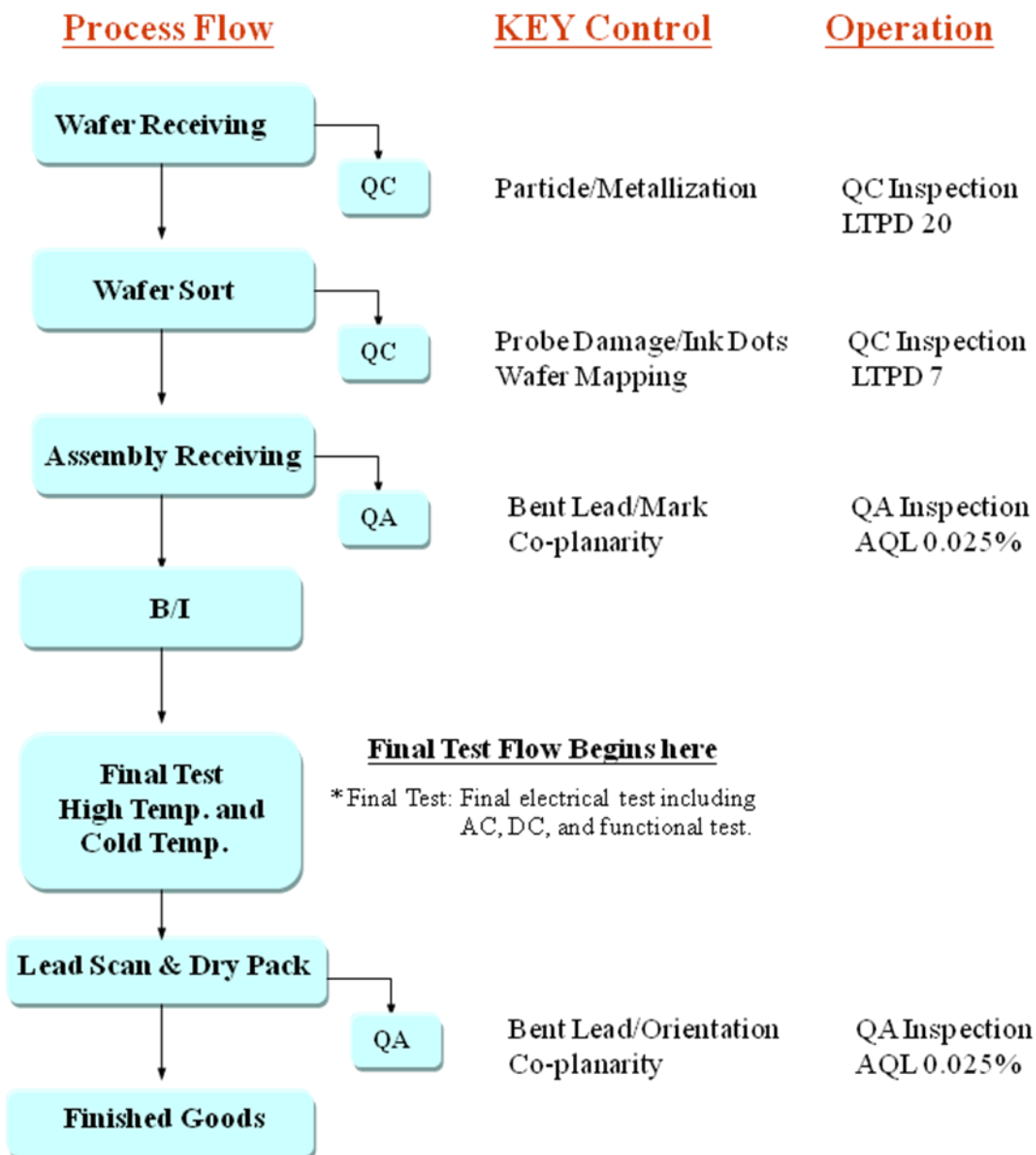


Figure 3-4 Commercial DRAM Test Flow & Control

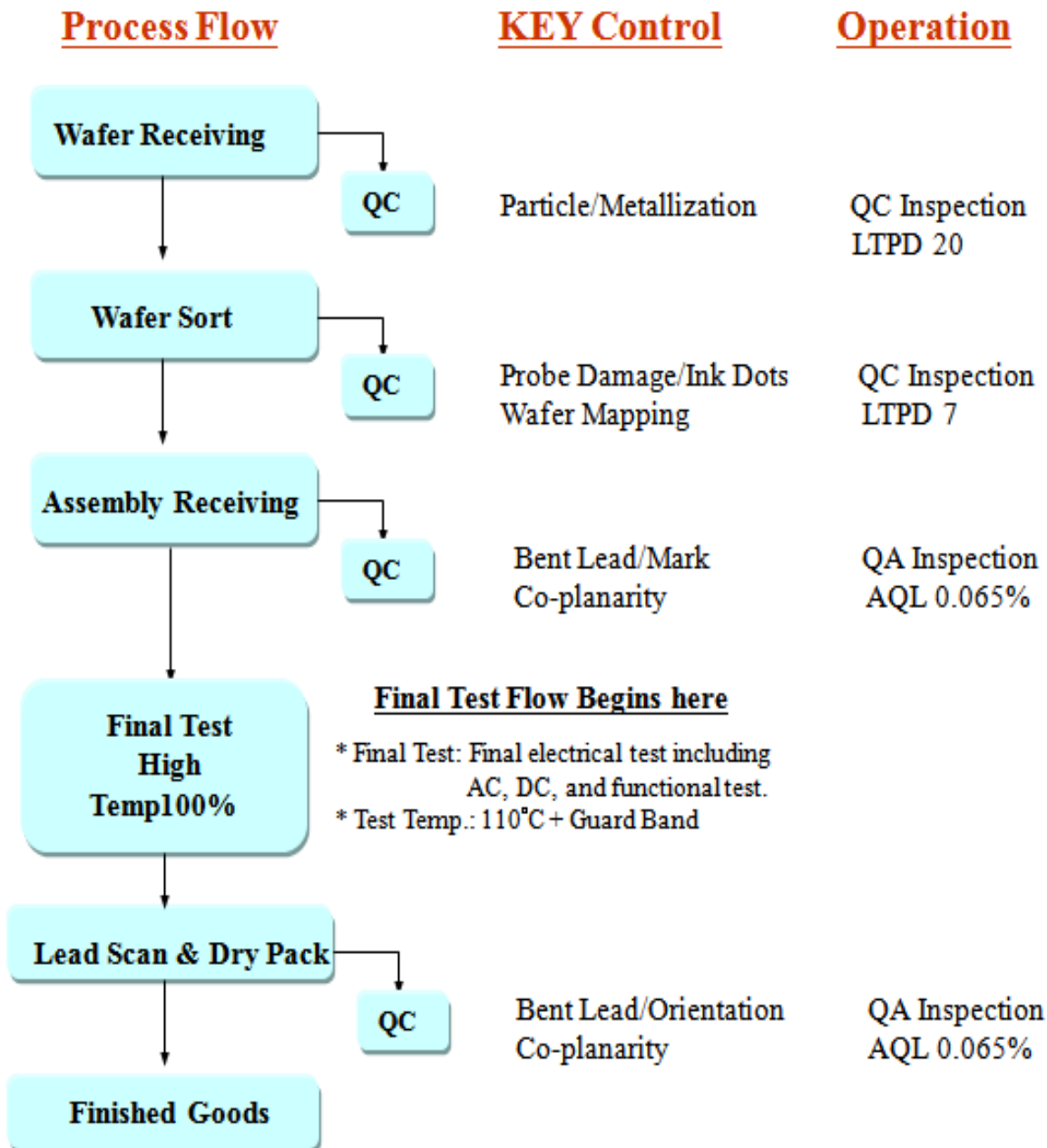


Figure 3-5 Commercial Flash Test Flow & Control

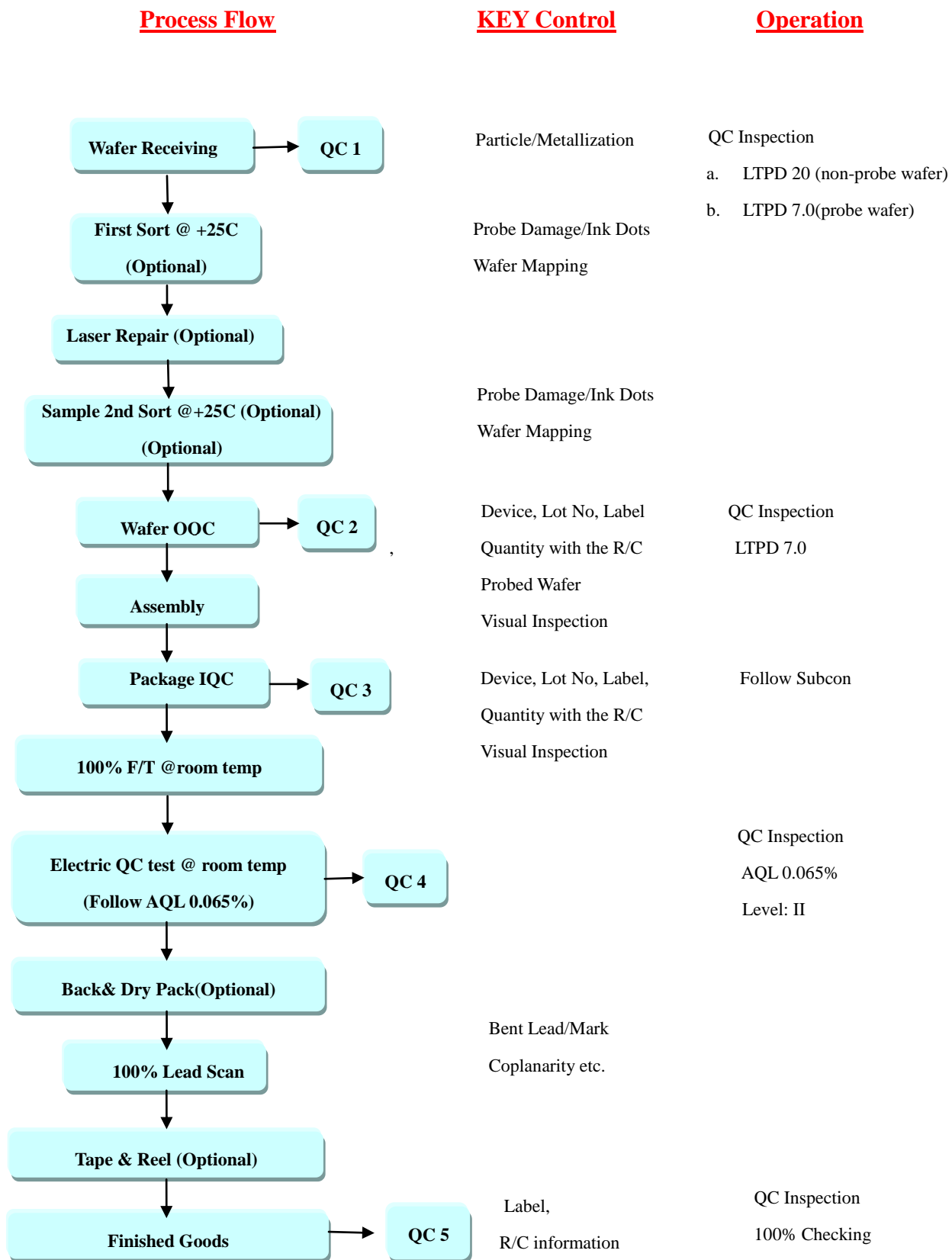


Figure 3-6 Commercial Analog Test Flow & Control

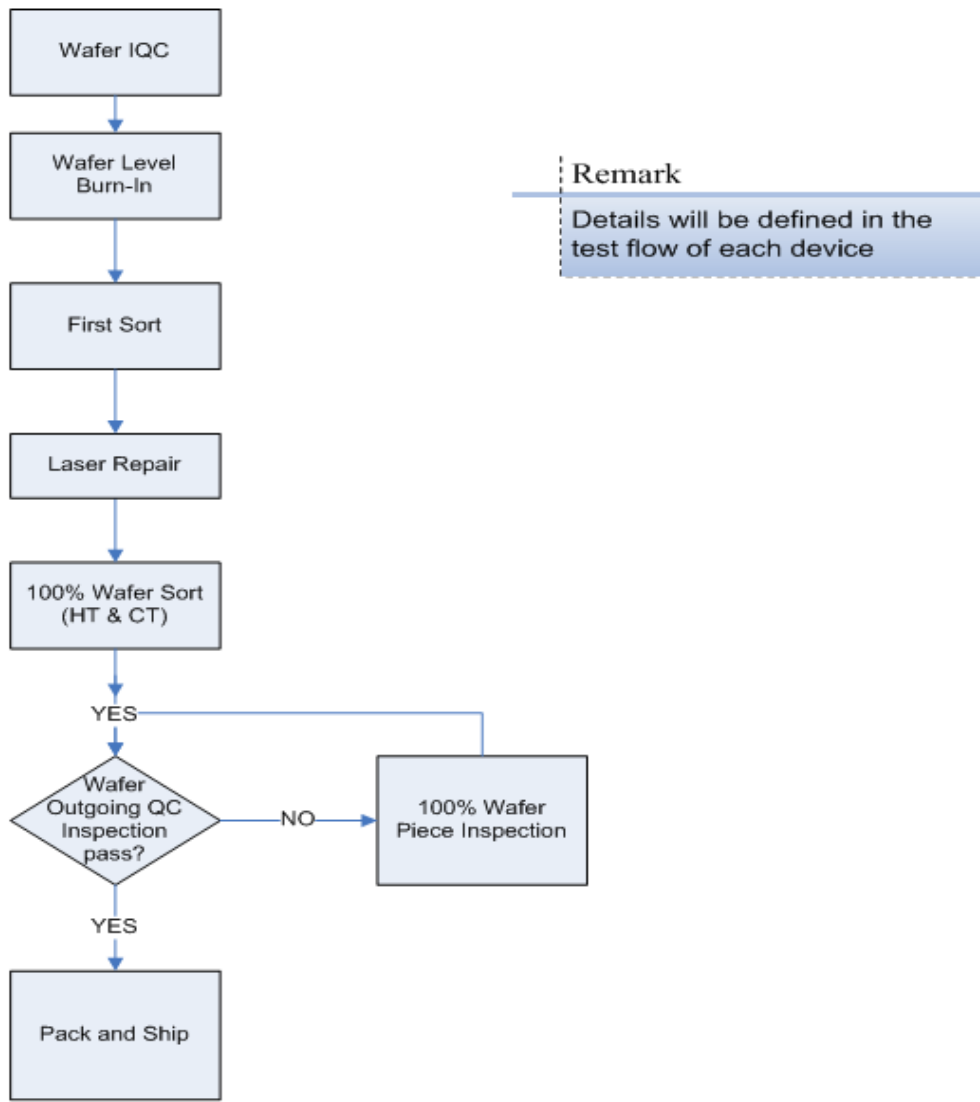


Figure 3-7 General Known Good Die Test Flow & Control

2.4 Quality Assurance of Product Shipping

Checks are carried out to ensure that the quality control established in the development and manufacturing stages is being reliably executed. Shipping inspections are performed to confirm the quality assurance of each lot in order to ensure the quality and reliability of shipped products.

The shipping inspection includes visual check and sampling of electrical characteristics. Visual check consists of checks on lead bending, marking defects, chipping, voids and defects. Electrical characteristics involve DC and AC characteristics as described in (section 3.2.5) "Monitoring Data for AOQL".

After the final inspection, judgment is made to confirm that the electrical specifications, appearance and packing condition of shipped products satisfy the specifications demanded by customers.

2.4.1 Monitoring Data for AOQL

ISSI establishes outgoing quality level target, measurement and procedure for continuous improvement.

- a) The target of outgoing quality level for ISSI products is less than 20 ppm for Memory and Analog products. This target is periodically reviewed by management representative to approach the goal of zero defects.
- b) All the device types will be measured to establish the outgoing quality level. QC shall issue quality discrepancy report (QDR) for the devices that fall below the targeted quality level and require analysis improvement until the desired quality level is achieved.
- c) The average outgoing quality level (AOQL) is sampled [from the ISSI inventory parts](#), and the sample lots should be included to be tested by each testing subcontractor.

Outgoing quality levels will be published by QRA and distributed to appropriate persons.

For Analog/Logic products, there are very few devices in stock and the AOQL is not monitored at present.