Serial RAM

- **Densities**: 8Mb, 16Mb, 32Mb, 64Mb
- **Packages**: 8-Pin SOIC, 8-Pin USON, 8-Pin WSON
- **Temperature**: -40 to 85°C; -40 to 105°C
- **On-Chip ECC**: Not Supported
- **Speed**: 104MHz (VDD = 1.7V - 1.95V) and (VDD = 2.7V - 3.6V)

OCTAL RAM

- **Densities**: 32Mb, 64Mb, 128Mb, 256Mb, 512Mb
- **Packages**: 24-Ball BGA
- **Temperature**: -40 to 85°C; -40 to 105°C; -40 to 125°C (64Mb, 128Mb)
- **On-Chip ECC**: On Chip ECC (2-bit detection, 1-bit correction) with optional ERR signal (64Mb, 128Mb)
- **Speed**: 200MHz (VDD = 1.7V - 1.95V) and 166MHz (VDD = 2.7V - 3.6V)

HYPER RAM™

- **Densities**: 64Mb, 128Mb, 256Mb, 512Mb
- **Packages**: 24-Ball BGA
- **Temperature**: -40 to 85°C; -40 to 105°C; -40 to 125°C (64Mb, 128Mb)
- **On-Chip ECC**: On Chip ECC (2-bit detection, 1-bit correction) with optional ERR signal (64Mb, 128Mb)
- **Speed**: 200MHz (VDD = 1.7V - 1.95V) and 166MHz (VDD = 2.7V - 3.6V)

Serial RAM Overview

- SPI (Serial Peripheral Interface) Compatible Bus: SPI(x1) / SDI(x2) / SQI(x4) mode
- Very Low Bus Signal Count: 6 pins for x4 IO; CS#, SCK, SI00 - SI03 or 4 pins for x1/x2 IO: CS#, SCK, SI[SI00], SO[SI01]
- Very Simple Commands [7 commands]: Read/Write Memory, Read/Write Register, Enter SDI (x2)/SQI mode(x4), and Return to SPI mode (x1)

Octal RAM Overview

- DRAM technology based solution with Hidden Refresh and OPI (Octal Peripheral Interface) Protocol
- Very Low Signal Count: 11(12) pins for Functions and 8 I/O. (Optional ERR# pin for 64Mb and 128Mb ECC products)
- Variable Latency or Fixed Latency, Burst Read/Write Operation and features Read Data Training (16-bit Pattern for Training Purpose)

HyperRAM™ Overview

- HyperRAM™ memory is DRAM based memory with HyperBus™ Interface
- Very Low Signal count (Address, Command, and Data through 8 DQ pins)
- Hidden Refresh operation
Low Pin Count RAM Solution

Targeting IoT, Automotive, Industrial & Other Applications

QUAD RAM Overview

- Quad DDR (x4 xSPI) Interface: Command (1 byte) = SDR, Address [2-byte] & Data = DDR
- Low Signal Counts: 7 Signal pins (CS#, SCLK, DQSM, SIO0~SIO3)
- Configurable Wrapped Burst Length: 16, 32, 64, and 128

Serial SRAM Overview

- Minimum four Signal Pins for 4Mb (x1): SI, SO, CK, CS#
- Random Read/Write Operation with Ultra Low Standby Current

QUAD RAM

- Densities: 8Mb, 16Mb, 32Mb, 64Mb
- Packages: 24-Ball BGA
- Temperature: -40 to 85°C; -40 to 105°C, -40 to 125°C (8Mb, 16Mb)
- On-Chip ECC: On Chip ECC (2-bit detection, 1-bit correction) with optional ERR signal in (8Mb, 16Mb)
- Speed: 200MHz (VDD = 1.7V - 1.95V)
  133MHz (VDD = 2.7V - 3.6V)

Serial SRAM

- Densities: 512Kb, 1Mb, 2Mb, 4Mb
- Packages: 8-Pin SOIC
- Temperature: -40 to 85°C; -40 to 105°C
- On-Chip ECC: Not Supported
- Speed: 30MHz (VDD = 1.65V - 2.2V)
  45MHz (VDD = 2.2V - 3.6V)

Low Pin Count RAM Solutions

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<tr>
<th>Low Pin Count</th>
<th>512Kb</th>
<th>1Mb</th>
<th>2Mb</th>
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<th>128Mb</th>
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Industrial & Automotive Temperature Grade, Long Term Support, RoHS & Halogen-free Compliance TSCA Compliance

STATUS

- Production
- Sampling
- In Development
- Under Consideration

ECC: On-chip Error Correcting Code is an available option